ZYNQ7000 FPGA

Development Board

AX7Z020B

User Manual

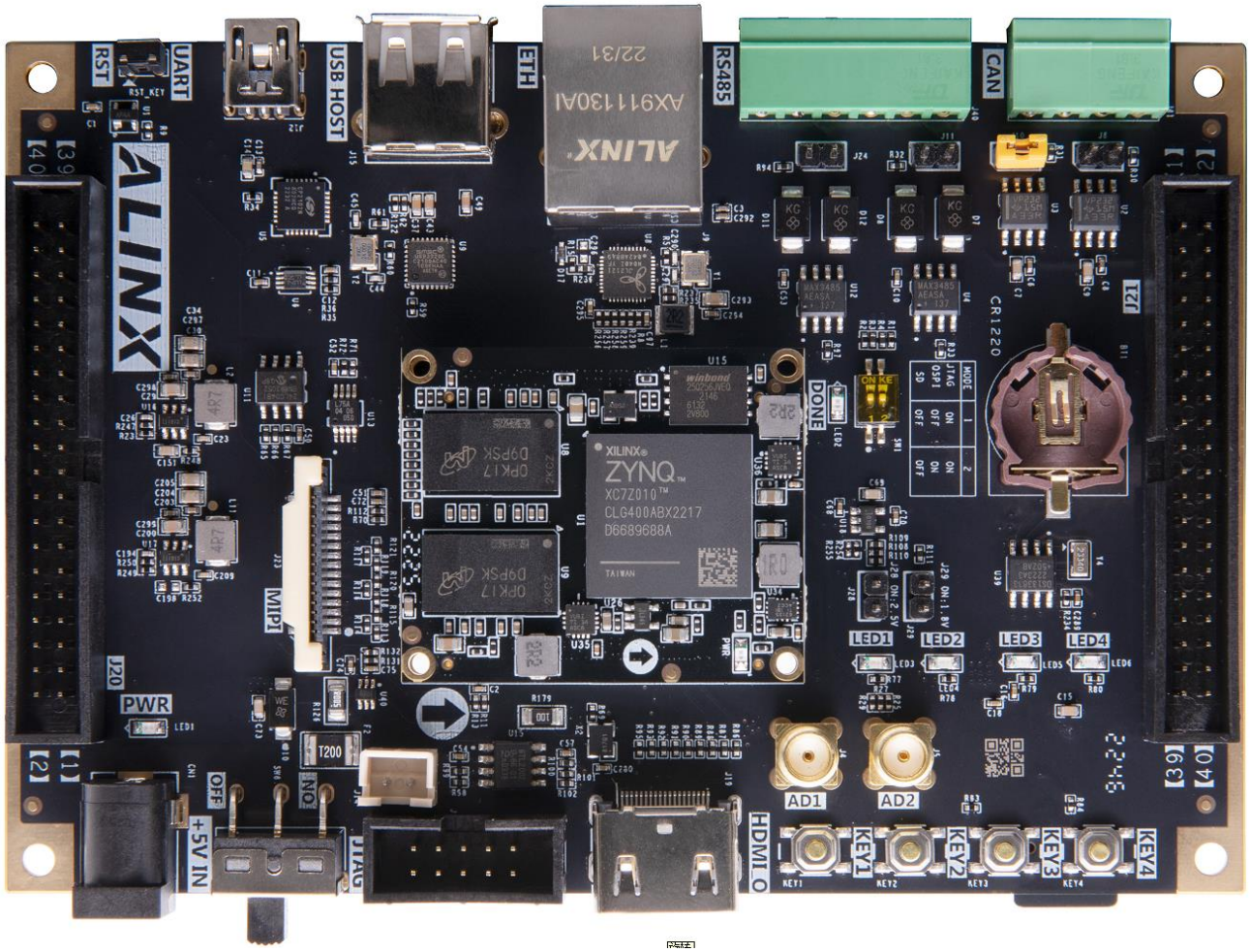
ALINX

Content

Based on XILINX ZYNQ7000 development platform, ALINX's development board AX7Z020B 2022 is officially released. This user manual is wrote in order to let users quickly understand this development platform.

This ZYNQ7000 FPGA development platform adopts the mode of core board and expansion board, which facilitates the secondary development and utilization of the core board. Its core board uses XILINX's Zynq7000 SOC chip solution, which uses ARM+FPGA SOC technology to integrate dual-core ARM Cortex-A9 and FPGA programmable logic on a single chip. In addition, the core board contains two high-speed DDR3 SDRAM chips with a total of 512MB and one 256Mb QSPI FLASH chip.

In the design of the carrier board, we have extended a variety of peripheral interfaces for users, such as 2 CAN communication interfaces, 2 485 communication interfaces, 2 XADC input interfaces, 1 Gigabit Ethernet interface, 1 USB2.0 HOST interface, 1 HDMI output interface, Uart communication interface, SD card holder, 40-pin expansion interface and so on. It is a "professional" ZYNQ development platform which can meet the user's requirements of various Ethernet high-speed data exchange, data storage, video transmission and processing as well as industrial control. It provides the possibility for high-speed Ethernet data transmission and exchange, the early verification and later application of data processing. We believe such a product would be ideal for students, engineers and other groups engaged in the development of ZYNQ.



1. Introduction

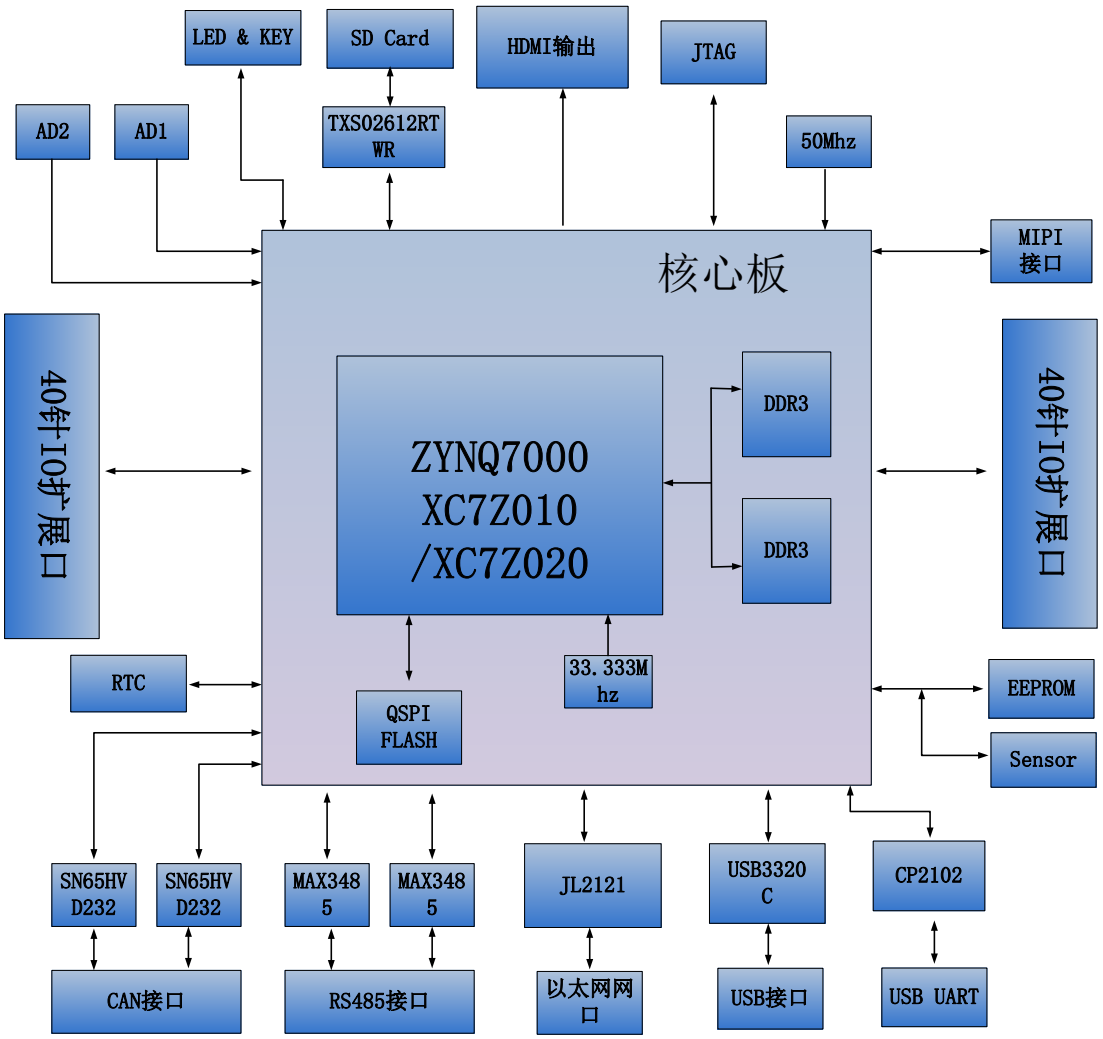
The entire structure of the development board is designed in core board+expansion board model. The core board and expansion board are connected using high-speed board-to-board connectors.

The core board is mainly composed of the XC7Z020 + 2 DDR3 + QSPI FLASH system, which is responsible for the high-speed data processing and storage functions of the ZYNQ system. The data bit width between ZYNQ7020 and two DDR3 chips is 32 bits, and the capacity of two DDR3 chips is up to 512MB. The ZYNQ7020 is based on Xilinx's Zynq7000 series chip, model XC7Z020-2CLG400I. It can be divided into a Processor System (PS) and a Programmable Logic (PL).

The carrier board extends rich peripheral interfaces for the core board, including one Gigabit Ethernet interface, one USB2.0 HOST interface, one HDMI output port, one SD Card interface, and one UART USB interface, 1 SD card interface, 1 MIPI

interface, 2 CAN bus interfaces, 2 RS485 bus interfaces, 2 AD input interfaces, 2 40-pin expansion interfaces and some key leds.

The following is the structure diagram of the whole development system:



Through this diagram, you can see the interfaces and functions that the AX7Z020B FPGA Development Board contains:

- ZYNQ7000 core board

The core board consists of XC7Z020+512MB DDR3+256Mb QSPI FLAS, and has an additional 33.333333MHz crystal oscillator provides the clock for the PS system.

- CAN communication interface

Two CAN bus interface, using TI SN65HVD232 chip.

- 485 communication interface

Two 485 communication interface, using MAX3485 chip of MAXIM company.

- Gigabit Ethernet interface

One 10/100M/1000M Ethernet RJ45 interface for Ethernet data exchange with

computers or other network devices. The network interface chip adopts JL2121 industrial-grade GPHY chip of JL Semiconductor Company.

- One high-speed USB2.0 HOST interface, which can be used to connect the development board to USB peripherals such as mouse, keyboard, and U disk;
- USB Uart interface

One Uart to USB interface for communicating with the computer, which is convenient for user debugging. The serial chip uses the USB-UAR chip of Silicon Labs CP2102GM, and the USB interface uses the MINI USB interface.

- Micro SD card holder

One Micro SD card holder used to store operating system images and file systems.

- D Analog input interface

Two AD analog input interfaces used for analog signal input and voltage conversion, SMA interface form. Analog signal voltage input range is 0~10V (do not input voltage beyond this range).

- One HDMI image and video output interface, which can achieve 1080P video image transmission;
- one IIC interface EEPROM 24LC04;
- An on-board temperature sensor chip LM75 is used to detect the ambient temperature of the board.
- One MIPI camera interface, which can connect to the OV5640 camera with the Alinx MIPI interface (used only by the AX7Z020B).
- One JTAG debugging interface.
- 40-pin expansion port

Two 40-pin 2.54mm pitch expansion ports can be connected to various modules of Alinx, such as binocular camera, TFT LCD screen, high-speed AD module, etc. The expansion port contains one 5V power supply, two 3.3V power supplies, three ground power supplies, and 34 I/O ports.

- LED

It has 7 LED leds in total, 1 on the core board, 6 on the carrier board. Among 6 LEDs on the carrier board, one is power indicator; one is DONE configuration indicator and 4 are user indicators. And the LED on the core board is a power indicator.

- Four user keys are installed on the carrier board.

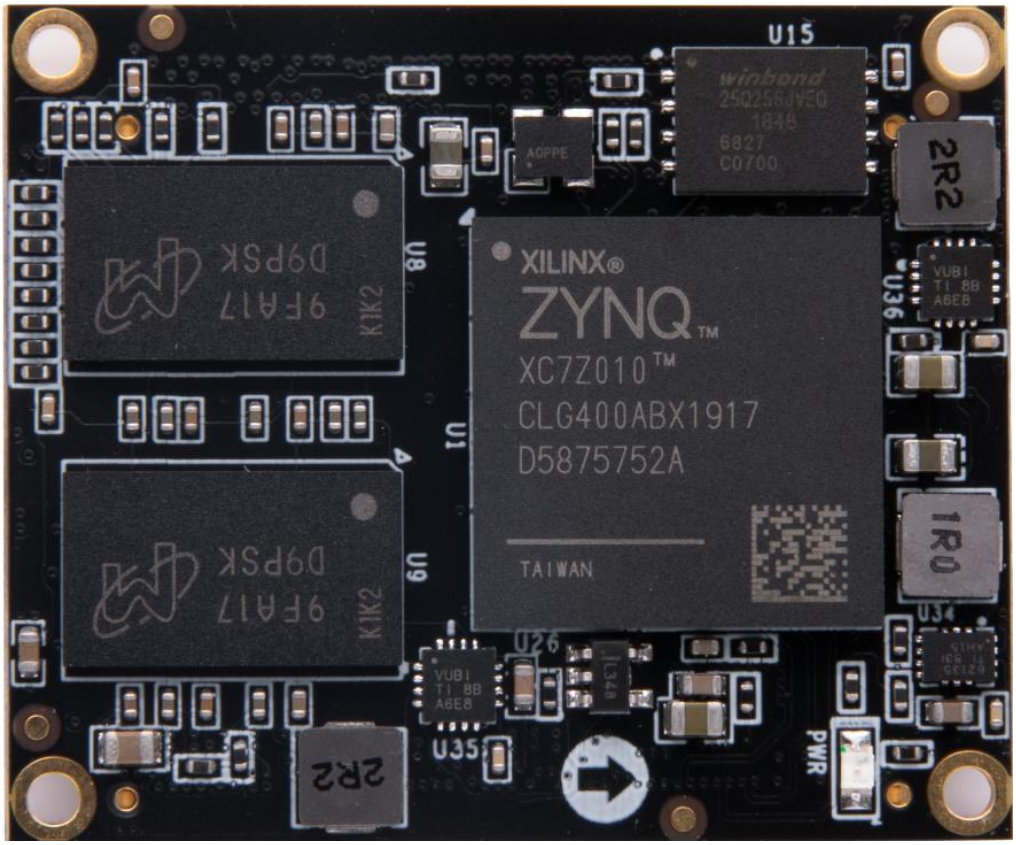
2. AC7Z020 Core Board

2.1 Introduction

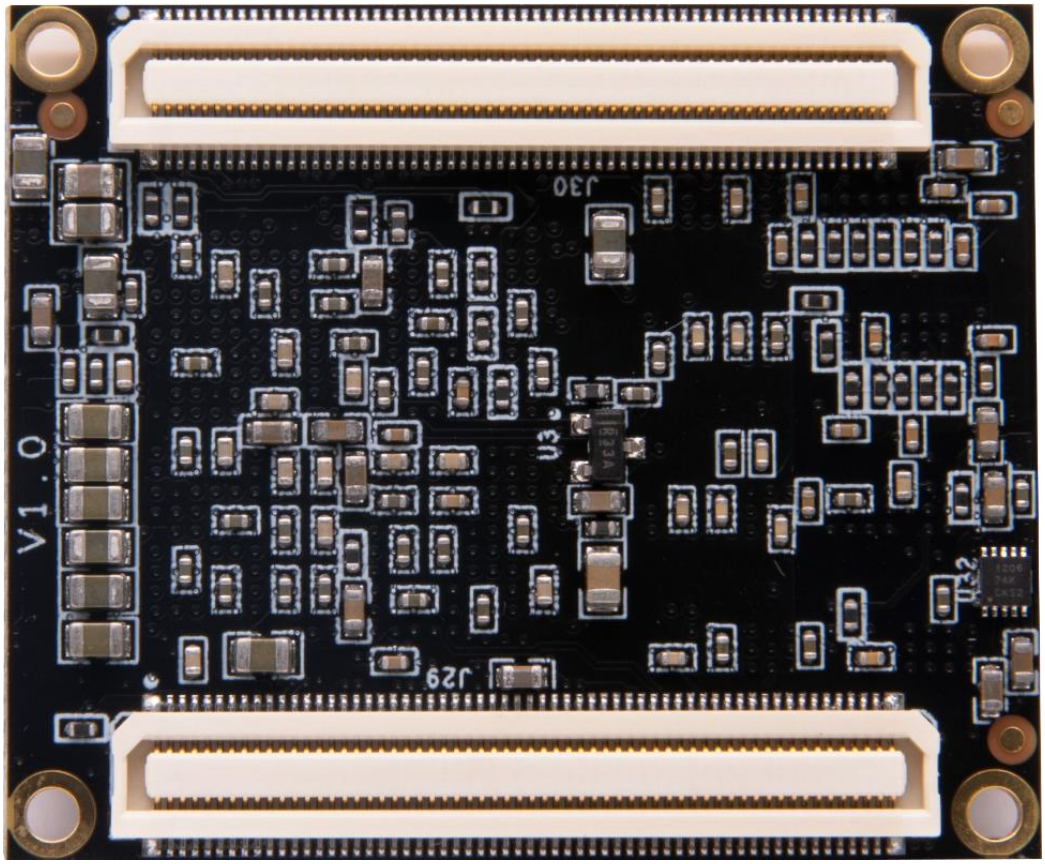
AC7Z020 (core board model, the same below) FPGA core board's ZYNQ chip is based on XC7Z020-2CLG400I of XILINX company ZYNQ7000 series. The ZYNQ chip's PS system integrates two ARM Cortex™-A9 processors, AMBA® interconnects, internal memory, external memory interfaces and peripherals. The FPGA of the ZYNQ chip contains a wealth of programmable logic cells, DSP and internal RAM.

This core board uses two Micron MT41K128M16TW-107 DDR3 chips, each DDR capacity of 256MB; Two DDR chips combine a 32bit data bus width, and the read/write data clock rate between ZYNQ and DDR3 is up to 533Mhz; Such configuration can meet the high bandwidth data processing requirements of the system.

In order to connect with the carrier board, 2 board-to-board connectors of the core board extend the USB interface, the Gigabit Ethernet interface, the SD card interface and other remaining IO ports (48) at the PS side; and also extend almost all IO ports (100) at the PL side, where the IO levels of BANK34 and BANK35 can be provided through the carrier board to meet the requirements of users with different level interfaces. For users who need a lot of IO, this core board will be a good choice. In addition, as for the IO connection part, the line between the ZYNQ chip and the interface is processed in equal length and differential length, and the core board size is only 35*42 (mm), which is very suitable for secondary development.



Front view of the AC7Z020 core board



Back view of the AC7Z020 core board

2.2 ZYNQ Chip

The development board uses Xilinx's Zynq7000 series chip, model XC7Z020-2CLG400I. The chip's PS system integrates two ARM Cortex™-A9 processors, AMBA® interconnects, internal memory, external memory interface, and peripherals. These peripherals mainly include USB bus interface, Ethernet interface, SD/SDIO interface, I2C bus interface, CAN bus interface, UART interface, GPIO and so on. PS can run independently and start in power-on or reset condition. Figure 2-2-1 shows the overall block diagram of the ZYNQ7000 chip:

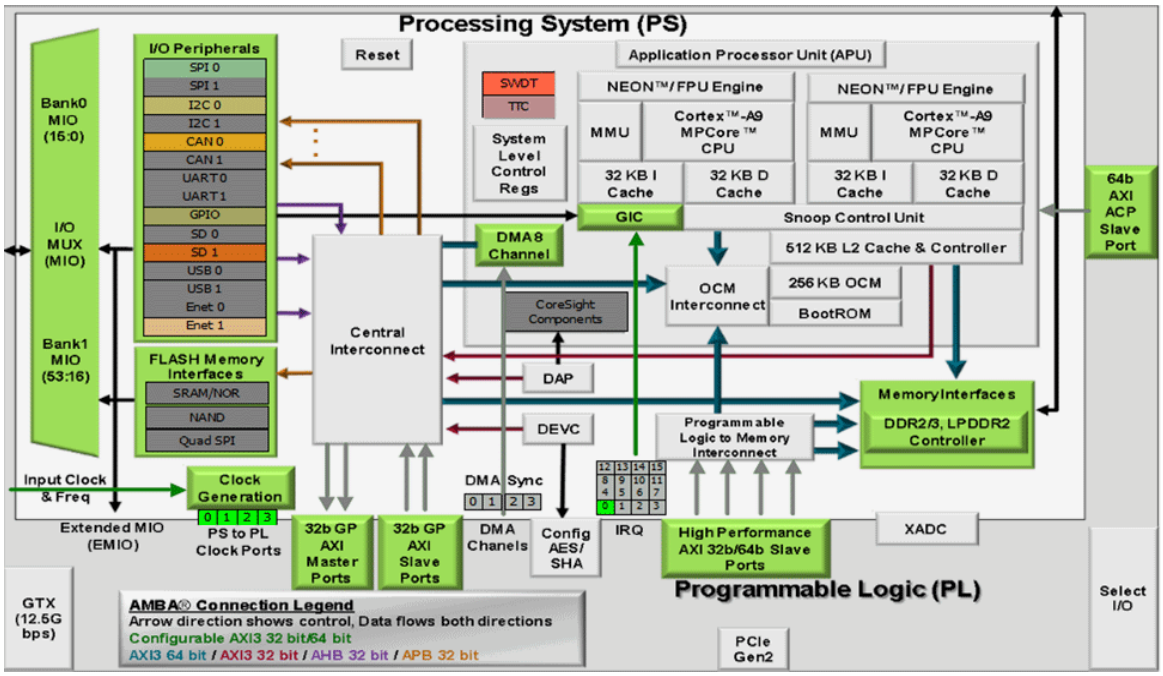


Figure 2-2-1 overall block diagram of ZYNQ7000 chip

The main parameters of the PS system are as follows:

- Application processor based on ARM dual-core CortexA9, and ARM-V7 architecture can up to 1GHz;
- 32KB Level 1 instruction and data cache per CPU, 512KB of level 2 cache shared by 2 CPUs;
- On-chip boot ROM and 256KB on-chip RAM;
- External storage interfaces, supporting 16/32 bit DDR2 and DDR3 interfaces;
- Two Gigabit Nics support: Divergence-aggregation DMA, GMII, RGMII, SGMII interfaces;
- Two USB2.0 OTG interfaces, each supporting a maximum of 12 nodes;
- Two CAN2.0B bus interfaces;
- Two SD cards, SDIO, MMC compatible controller;

- Two SPI, two UARTs, two I2C interfaces;
- 4 sets of 32bit GPIO, 54 (32+22) as PS system IO, 64 connected to PL;
- High bandwidth connections within PS and PS to PL.

The main parameters of the PL logic are as follows:

- Logic Cells：85K；
- LUTs: 53,200
- Flip-flops:106,400
- Multiplier 18x25MACCs：220;
- Block RAM：4.9Mb；
- Two AD converters that can measure on-chip voltage, temperature sensing and up to 17 external differential input channels at 1MBPS

XC7Z020-2CLG400I chip speed grade is -2, industrial grade, package is BGA400, pin spacing is 0.8mm. Specific definition of chip model of ZYNQ7000 series is shown in Figure 2-2-2 below.

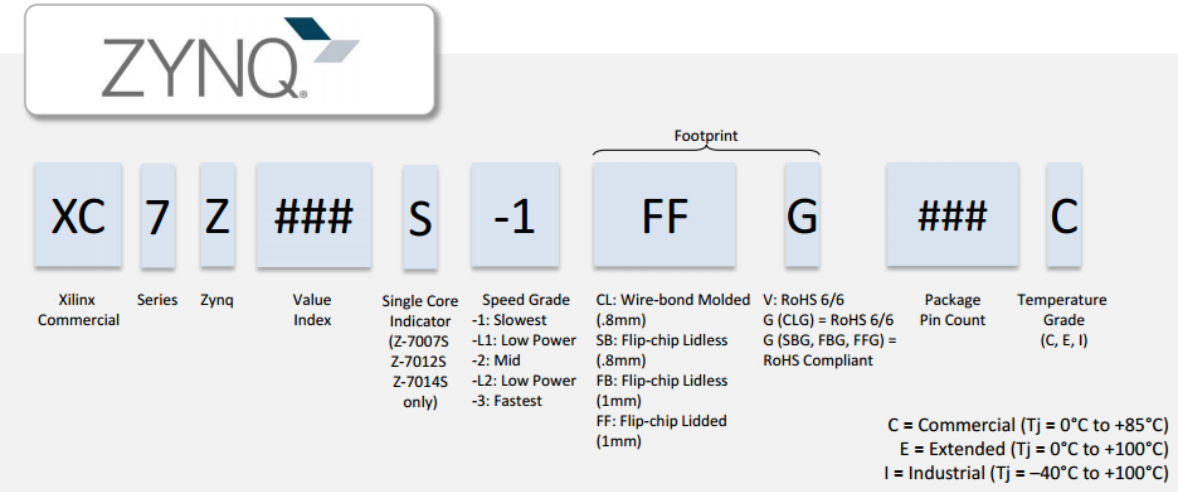


Figure 2-2-2 Naming definition of ZYNQ model

2.3 DDR3 DRAM

The AC7Z020 core board is equipped with two Micron DDR3 SDRAM chips (1GB in total), model MT41K256M16TW-107 (compatible with Hynix H5TQ4G63AFR-PBI). DDR3 SDRAM has a total bus width of 32 bits and operates at a maximum speed of 533MHz (1066Mbps data rate). The DDR3 storage system is directly connected to the memory interface of the BANK 502 of the ZYNQ processing system (PS). The DDR3

SDRAM configuration is shown in Table 2-3-1 below.

Table 2-3-1 DDR3 SDRAM Configuration

Position	Chip Model	Capacity	Factory
U8,U9	MT41K256M16TW-107	256M x 16bit	Micron

The hardware design of DDR3 requires strict consideration of signal integrity. We have fully considered the matching resistor/terminal resistance, trace impedance control, and line length control in circuit design and PCB design to ensure high-speed and stable operation of DDR3.

DDR3 DRAM hardware connection is shown in Figure 2-3-1:

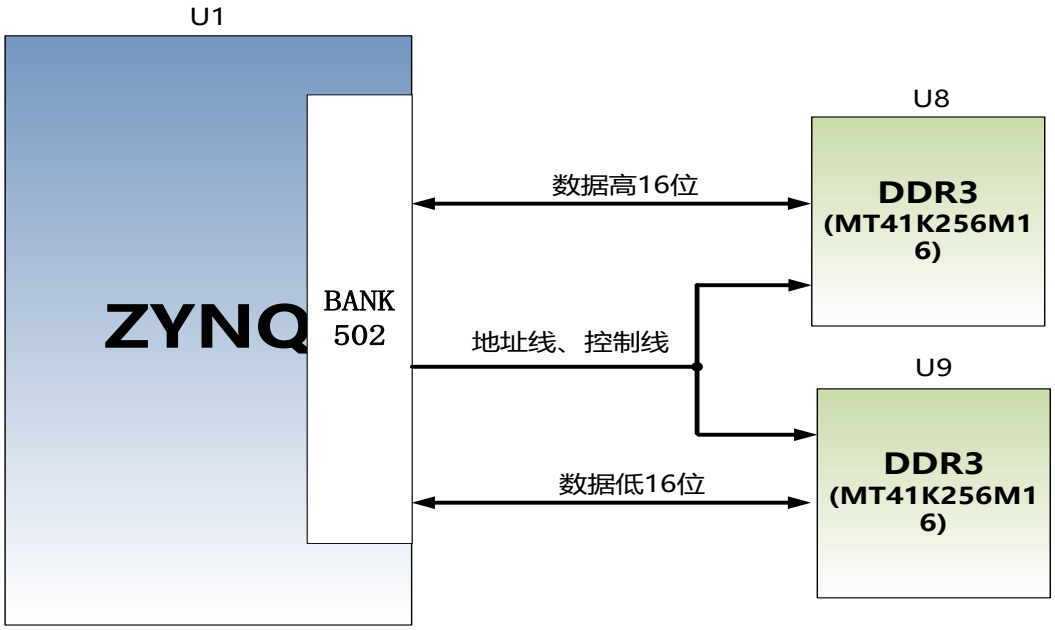


Figure 2-3-1 DDR3 DRAM schematic diagram

DDR3 DRAM pin assignment:

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number
DDR3_DQS0_P	PS_DDR_DQS_P0_502	C2
DDR3_DQS0_N	PS_DDR_DQS_N0_502	B2
DDR3_DQS1_P	PS_DDR_DQS_P1_502	G2
DDR3_DQS1_N	PS_DDR_DQS_N1_502	F2
DDR3_DQS2_P	PS_DDR_DQS_P2_502	R2
DDR3_DQS2_N	PS_DDR_DQS_N2_502	T2
DDR3_DQS3_P	PS_DDR_DQS_P3_502	W5

DDR3_DQS4_N	PS_DDR_DQS_N3_502	W4
DDR3_D0	PS_DDR_DQ0_502	C3
DDR3_D1	PS_DDR_DQ1_502	B3
DDR3_D2	PS_DDR_DQ2_502	A2
DDR3_D3	PS_DDR_DQ3_502	A4
DDR3_D4	PS_DDR_DQ4_502	D3
DDR3_D5	PS_DDR_DQ5_502	D1
DDR3_D6	PS_DDR_DQ6_502	C1
DDR3_D7	PS_DDR_DQ7_502	E1
DDR3_D8	PS_DDR_DQ8_502	E2
DDR3_D9	PS_DDR_DQ9_502	E3
DDR3_D10	PS_DDR_DQ10_502	G3
DDR3_D11	PS_DDR_DQ11_502	H3
DDR3_D12	PS_DDR_DQ12_502	J3
DDR3_D13	PS_DDR_DQ13_502	H2
DDR3_D14	PS_DDR_DQ14_502	H1
DDR3_D15	PS_DDR_DQ15_502	J1
DDR3_D16	PS_DDR_DQ16_502	P1
DDR3_D17	PS_DDR_DQ17_502	P3
DDR3_D18	PS_DDR_DQ18_502	R3
DDR3_D19	PS_DDR_DQ19_502	R1
DDR3_D20	PS_DDR_DQ20_502	T4
DDR3_D21	PS_DDR_DQ21_502	U4
DDR3_D22	PS_DDR_DQ22_502	U2
DDR3_D23	PS_DDR_DQ23_502	U3
DDR3_D24	PS_DDR_DQ24_502	V1
DDR3_D25	PS_DDR_DQ25_502	Y3
DDR3_D26	PS_DDR_DQ26_502	W1
DDR3_D27	PS_DDR_DQ27_502	Y4
DDR3_D28	PS_DDR_DQ28_502	Y2
DDR3_D29	PS_DDR_DQ29_502	W3
DDR3_D30	PS_DDR_DQ30_502	V2

DDR3_D31	PS_DDR_DQ31_502	V3
DDR3_DM0	PS_DDR_DM0_502	A1
DDR3_DM1	PS_DDR_DM1_502	F1
DDR3_DM2	PS_DDR_DM2_502	T1
DDR3_DM3	PS_DDR_DM3_502	Y1
DDR3_A0	PS_DDR_A0_502	N2
DDR3_A1	PS_DDR_A1_502	K2
DDR3_A2	PS_DDR_A2_502	M3
DDR3_A3	PS_DDR_A3_502	K3
DDR3_A4	PS_DDR_A4_502	M4
DDR3_A5	PS_DDR_A5_502	L1
DDR3_A6	PS_DDR_A6_502	L4
DDR3_A7	PS_DDR_A7_502	K4
DDR3_A8	PS_DDR_A8_502	K1
DDR3_A9	PS_DDR_A9_502	J4
DDR3_A10	PS_DDR_A10_502	F5
DDR3_A11	PS_DDR_A11_502	G4
DDR3_A12	PS_DDR_A12_502	E4
DDR3_A13	PS_DDR_A13_502	D4
DDR3_A14	PS_DDR_A14_502	F4
DDR3_BA0	PS_DDR_BA0_502	L5
DDR3_BA1	PS_DDR_BA1_502	R4
DDR3_BA2	PS_DDR_BA2_502	J5
DDR3_S0	PS_DDR_CS_B_502	N1
DDR3_RAS	PS_DDR_RAS_B_502	P4
DDR3_CAS	PS_DDR_CAS_B_502	P5
DDR3_WE	PS_DDR_WE_B_502	M5
DDR3_ODT	PS_DDR_ODT_502	N5
DDR3_RESET	PS_DDR_DRST_B_502	B4
DDR3_CLK0_P	PS_DDR_CKP_502	L2
DDR3_CLK0_N	PS_DDR_CKN_502	M2
DDR3_CKE	PS_DDR_CKE_502	N3

2.4 QSPI Flash

The FPGA core board is equipped with a 256MBit Quad-SPI FLASH chip (model: W25Q256FVEI), which uses the 3.3V CMOS voltage standard. Due to the non-volatile characteristics of QSPI FLASH, it can be used as the boot device of the system to store the boot image of the system. These images mainly include FPGA bit files, ARM application code, and other user data files. The specific models and related parameters of QSPI FLASH are shown in Table 2-4-1.

Position	Model	Capacity	Factory
U15	W25Q256FVEI	32M Byte	Winbond

Table 2-4-1 Model and parameter of QSPI Flash

The QSPI FLASH is connected to the GPIO port of the PS part BANK500 of the ZYNQ chip. In the system design, the GPIO port of the PS side needs to be configured as the QSPI FLASH interface. Figure 2-4-1 shows the part of QSPI Flash in the schematic.

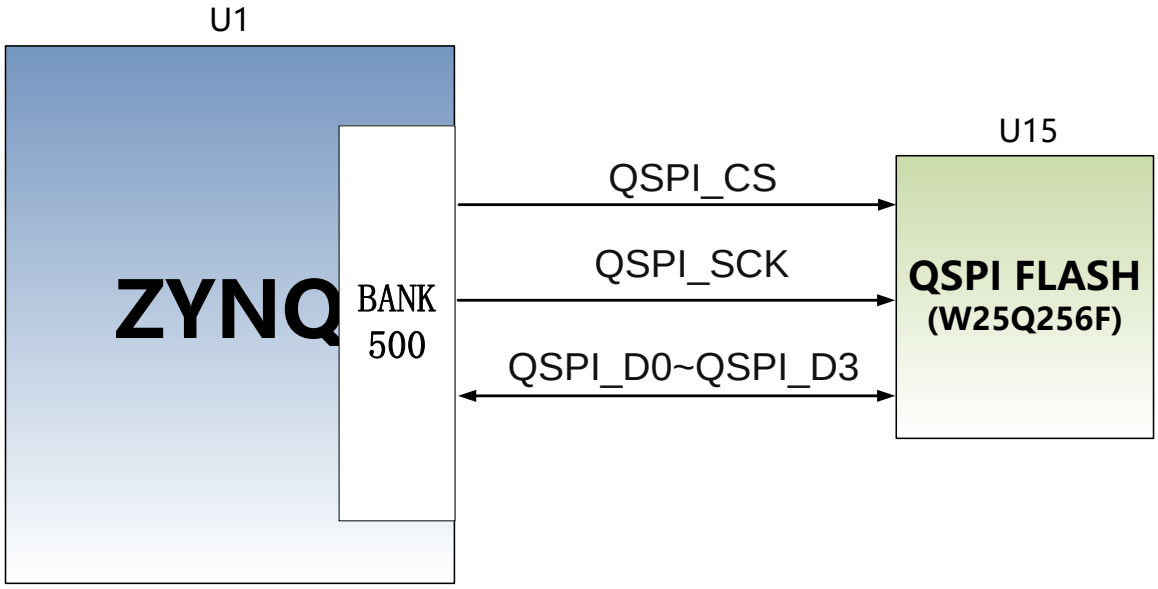


Figure 2-4-1 Connection diagram of QSPI Flash

Configuration chip pin assignment:

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number
QSPI_SCK	PS_MIO6_500	A5
QSPI_CS	PS_MIO1_500	A7
QSPI_D0	PS_MIO2_500	B8
QSPI_D1	PS_MIO3_500	D6
QSPI_D2	PS_MIO4_500	B7
QSPI_D3	PS_MIO5_500	A6

2.5 Configuration of Clock

The AC7Z020 core board provides an active clock for the PS system, so that the PS system can work independently. The reference clock on the PL side is provided by the carrier board.

PS System Clock Source

The ZYNQ chip provides 33.333333MHz clock input to the PS through the X1 crystal oscillator on the core board. The input of the clock is connected to the pin of the PS_CLK_500 of the BANK500 of the ZYNQ chip. Figure 2-5-1shows its schematic diagram:

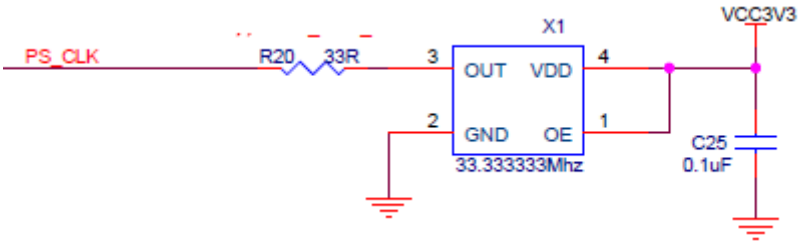


Figure 2-5-1 The active crystal oscillator of the PS

Clock pin assignment:

Signal Name	ZYNQ Pin
PS_CLK_500	E7

PL System Clock Source

The PL clock needs to be provided through the carrier board, and there is a 50Mhz clock on the AX7Z020B carrier board to provide clock reference for the PL system. The input of the clock is connected to the pin of the BANK34 U18 of the

ZYNQ chip. Figure 2-5-2 shows its schematic diagram:

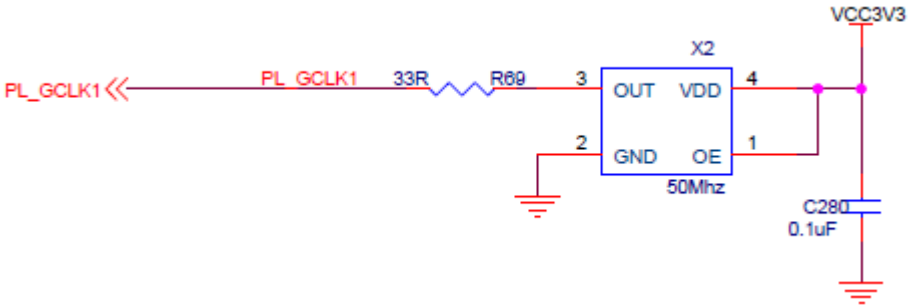


Figure 2-5-2 The crystal oscillator of the PL on the carrier board

Clock pin assignment:

Signal Name	ZYNQ Pin
PL_GCLK1	U18

2.6 Power Supply

The power supply voltage of AC7Z020 core board is DC5V, which is supplied by connecting to the carrier board. In addition, the power supply of BANK34 and BANK35 is also provided by the carrier board. Figure 2-6-1 shows the design of power supply on the board:

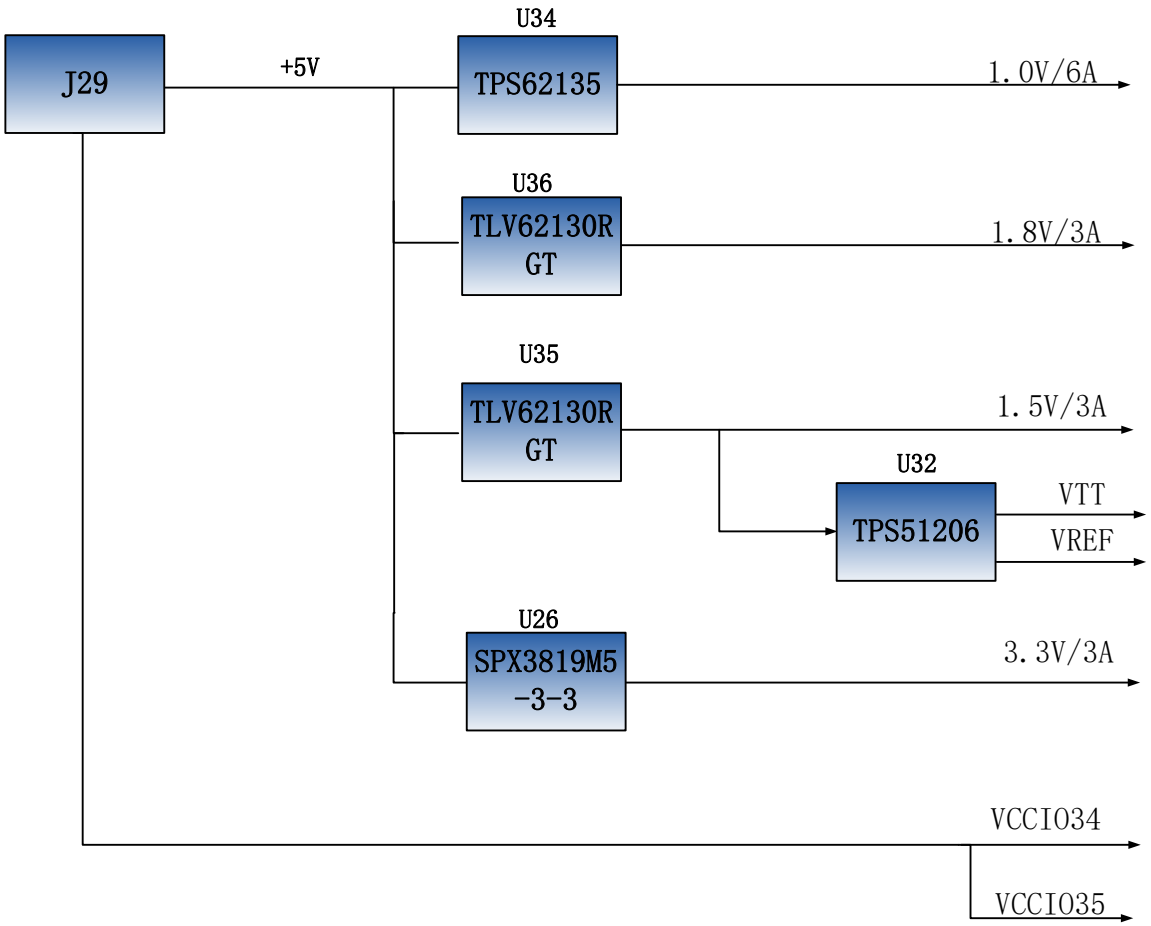


Figure 2-6-1 Schematic diagram of the power interface

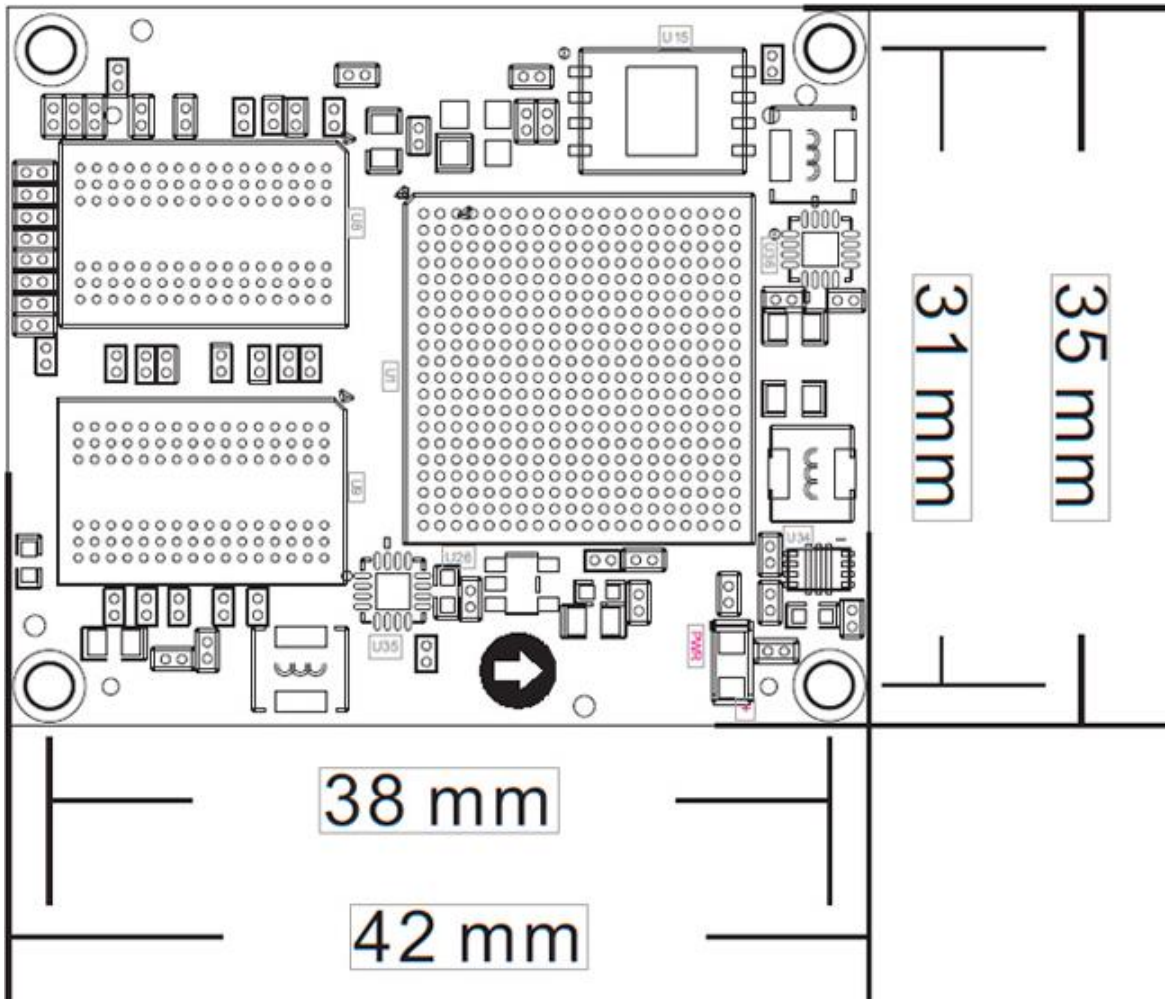
The development board is powered by +5V, converted into four-channel power supplies (+1.0V, +1.8V, +1.5V, +3.3V) through four-channel DC/DC power chips. +1.0V output current can be up to 6A, +1.8V and +1.5V power supply is 3A, +3.3V is 500mA. The J29 also has four pins each to supply power to the BANK34 and BANK35 of the FPGA (3.3V as default), and users can change the power supply of the BANK34 and BANK35 by changing the VCCIO34 and VCCIO35 on the carrier board. 1.5V generates the VTT and VREF voltages required for DDR3 through TI's TPS51206. The functions of each power distribution are shown in the following table:

Power	Function
+1.0V	Kernel voltage of ZYNQ PS and PL parts
+1.8V	Auxiliary voltage of ZYNQ PS and PL parts, BANK501 IO voltage
+3.3V	ZYNQ Bank0,Bank500，QSIP FLASH, Clock crystal oscillator

+1.5V	DDR3, ZYNQ Bank501
VREF, VTT （+0.75V）	DDR3
VCCIO34/35	Bank34, Bank35

Because the power supply of ZYNQ FPGA has the requirements of power-on sequence, so that when designing the circuit, we have already designed according to the power supply requirements of the chip, and the circuit design is +1.0V->+1.8V->(+ 1.5V, +3.3V, VCCIO) to ensure the normal operation of the chip. Because level standard of BANK34 and BANK35 is determined by the power supply provided by the carrier board (3.3V as the maximum), so when users designing the VCCIO34 and VCCIO35 power supplied to the core board by the carrier board, the power-on sequence should slower than +5V.

2.7 Structure Diagram



Front View

2.8 Board to Board Connectors Pin Assignment

The core board has a total of two high-speed expansion ports, using two 120-pin board-to-board connectors (J29/J30) to connect to the carrier board, and the PIN spacing of connectors is 0.5mm. Among them, J29 is connected to 5V power supply, VCCIO power input, some IO signals and JTAG signals, and the J30 is connected to the remaining IO signal and MIO. The IO level of BANK34 and BANK35 can be changed by adjusting the VCCIO input on the connector, the highest level does not exceed 3.3V. The AX7Z020B carrier board we designed is 3.3V by default. **Note that the IO of BANK13 is not available for AC7Z020 core board.**

J29 connector pin assignment:

J29 Pin	Signal Name	ZYNQ Pin NO.	J29 Pin	Signal Name	ZYNQ Pin No.
1	VCC5V	-	2	VCC5V	-
3	VCC5V	-	4	VCC5V	-
5	VCC5V	-	6	VCC5V	-
7	VCC5V	-	8	VCC5V	-
9	GND	-	10	GND	-
11	VCCIO_34	-	12	VCCIO_35	-
13	VCCIO_34	-	14	VCCIO_35	-
15	VCCIO_34	-	16	VCCIO_35	-
17	VCCIO_34	-	18	VCCIO_35	-
19	GND	-	20	GND	-
21	IO34_L10P	V15	22	IO34_L7P	Y16
23	IO34_L10N	W15	24	IO34_L7N	Y17
25	IO34_L15N	U20	26	IO34_L17P	Y18
27	IO34_L15P	T20	28	IO34_L17N	Y19
29	GND	-	30	GND	-
31	IO34_L9N	U17	32	IO34_L8P	W14
33	IO34_L9P	T16	34	IO34_L8N	Y14
35	IO34_L12N	U19	36	IO34_L3P	U13
37	IO34_L12P	U18	38	IO34_L3N	V13

39	GND	-	40	GND	-
41	IO34_L14N	P20	42	IO34_L21N	V18
43	IO34_L14P	N20	44	IO34_L21P	V17
45	IO34_L16N	W20	46	IO34_L18P	V16
47	IO34_L16P	V20	48	IO34_L18N	W16
49	GND	-	50	GND	-
51	IO34_L22N	W19	52	IO34_L23P	N17
53	IO34_L22P	W18	54	IO34_L23N	P18
55	IO34_L20N	R18	56	IO34_L13N	P19
57	IO34_L20P	T17	58	IO34_L13P	N18
59	GND	-	60	GND	-
61	IO34_L19N	R17	62	IO34_L11N	U15
63	IO34_L19P	R16	64	IO34_L11P	U14
65	IO34_L24P	P15	66	IO34_L5N	T15
67	IO34_L24N	P16	68	IO34_L5P	T14
69	GND	-	70	GND	-
71	IO34_L4P	V12	72	IO34_L2N	U12
73	IO34_L4N	W13	74	IO34_L2P	T12
75	IO34_L1P	T11	76	IO34_L6N	R14
77	IO34_L1N	T10	78	IO34_L6P	P14
79	GND	-	80	GND	-
81	IO13_L13P	Y7	82	IO13_L21P	V11
83	IO13_L13N	Y6	84	IO13_L21N	V10
85	IO13_L11N	V7	86	IO13_L14N	Y8
87	IO13_L11P	U7	88	IO13_L14P	Y9
89	GND	-	90	GND	-
91	IO13_L19N	U5	92	IO13_L22N	W6
93	IO13_L19P	T5	94	IO13_L22P	V6
95	IO13_L16P	W10	96	IO13_L15P	V8
97	IO13_L16N	W9	98	IO13_L15N	W8
99	GND	-	100	GND	-
101	IO13_L17P	U9	102	IO13_L20P	Y12

103	IO13_L17N	U8	104	IO13_L20N	Y13
105	IO13_L18P	W11	106	IO13_L12N	U10
107	IO13_L18N	Y11	108	IO13_L12P	T9
109	GND	-	110	GND	-
111	FPGA_TCK	F9	112	VP	K9
113	FPGA_TMS	J6	114	VN	L10
115	FPGA_TDO	F6	116	PS_POR_B	C7
117	FPGA_TDI	G6	118	FPGA_DONE	R11
119	NC	-	120	NC	-

J30 connector pin assignment:

J30 Pin	Signal Name	ZYNQ Pin No.	J30 Pin	Signal Name	ZYNQ Pin No.
1	IO35_L1P	C20	2	IO35_L15N	F20
3	IO35_L1N	B20	4	IO35_L15P	F19
5	IO35_L18N	G20	6	IO35_L5P	E18
7	IO35_L18P	G19	8	IO35_L5N	E19
9	GND	T13	10	GND	T13
11	IO35_L10N	J19	12	IO35_L3N	D18
13	IO35_L10P	K19	14	IO35_L3P	E17
15	IO35_L2N	A20	16	IO35_L4P	D19
17	IO35_L2P	B19	18	IO35_L4N	D20
19	GND	T13	20	GND	T13
21	IO35_L8P	M17	22	IO35_L9N	L20
23	IO35_L8N	M18	24	IO35_L9P	L19
25	IO35_L7P	M19	26	IO35_L6P	F16
27	IO35_L7N	M20	28	IO35_L6N	F17
29	GND	T13	30	GND	T13
31	IO35_L17N	H20	32	IO35_L16N	G18
33	IO35_L17P	J20	34	IO35_L16P	G17
35	IO35_L19N	G15	36	IO35_L13N	H17

37	IO35_L19P	H15	38	IO35_L13P	H16
39	GND	T13	40	GND	T13
41	IO35_L12N	K18	42	IO35_L14N	H18
43	IO35_L12P	K17	44	IO35_L14P	J18
45	IO35_L24N	J16	46	IO35_L20P	K14
47	IO35_L24P	K16	48	IO35_L20N	J14
49	GND	T13	50	GND	T13
51	IO35_L21N	N16	52	IO35_L11P	L16
53	IO35_L21P	N15	54	IO35_L11N	L17
55	IO35_L22N	L15	56	IO35_L23P	M14
57	IO35_L22P	L14	58	IO35_L23N	M15
59	GND	T13	60	GND	T13
61	PS_MIO22	B17	62	PS_MIO50	B13
63	PS_MIO27	D13	64	PS_MIO45	B15
65	PS_MIO23	D11	66	PS_MIO46	D16
67	PS_MIO24	A16	68	PS_MIO41	C17
69	GND	T13	70	GND	T13
71	PS_MIO25	F15	72	PS_MIO7	D8
73	PS_MIO26	A15	74	PS_MIO12	D9
75	PS_MIO21	F14	76	PS_MIO10	E9
77	PS_MIO16	A19	78	PS_MIO11	C6
79	GND	T13	80	GND	T13
81	PS_MIO20	A17	82	PS_MIO9	B5
83	PS_MIO19	D10	84	PS_MIO14	C5
85	PS_MIO18	B18	86	PS_MIO8	D5
87	PS_MIO17	E14	88	PS_MIO0	E6
89	GND	T13	90	GND	T13
91	PS_MIO39	C18	92	PS_MIO13	E8
93	PS_MIO38	E13	94	PS_MIO47	B14
95	PS_MIO37	A10	96	PS_MIO48	B12
97	PS_MIO28	C16	98	PS_MIO49	C12
99	GND	T13	100	GND	T13

101	PS_MIO35	F12	102	PS_MIO52	C10
103	PS_MIO34	A12	104	PS_MIO51	B9
105	PS_MIO33	D15	106	PS_MIO40	D14
107	PS_MIO32	A14	108	PS_MIO44	F13
109	GND	T13	110	GND	T13
111	PS_MIO31	E16	112	PS_MIO15	C8
113	PS_MIO36	A11	114	PS_MIO42	E12
115	PS_MIO29	C13	116	PS_MIO43	A9
117	PS_MIO30	C15	118	PS_MIO53	C11
119	QSPI_D3_PS_MIO5	A6	120	QSPI_D2_PS_MIO4	B7

3. Carrier Board

3.1 Introduction

After introducing functions above, you can learn the function of the carrier board:

- 2 CAN communication interfaces
- 2 485 communication interfaces
- 1 10/100M/1000M Ethernet RJ-45 interface
- 1 USB HOST interface
- 1 USB Uart communication interface
- 1 SD card slot
- 2 40-pin expansion ports
- 2 AD input interfaces
- 1 HDMI video output interface
- 1 MIPI camera interface (only for AX7Z020B)
- 1 RTC real-time clock
- 1 EEPROM
- 1 temperature sensor
- JTAG debugging interface
- 4 independent keys

- 4 user LED lights

3.2 CAN Communication Interface

There are 2 CAN communication interfaces on the AX7Z020B carrier board, which are connected to the GPIO interface of the BANK500 on the PS system side. The CAN transceiver chip selected TI's SN65HVD232C chip for user CAN communication services.

Figure 3-2-1 shows the connection diagram of of CAN transceiver chip on PS side:

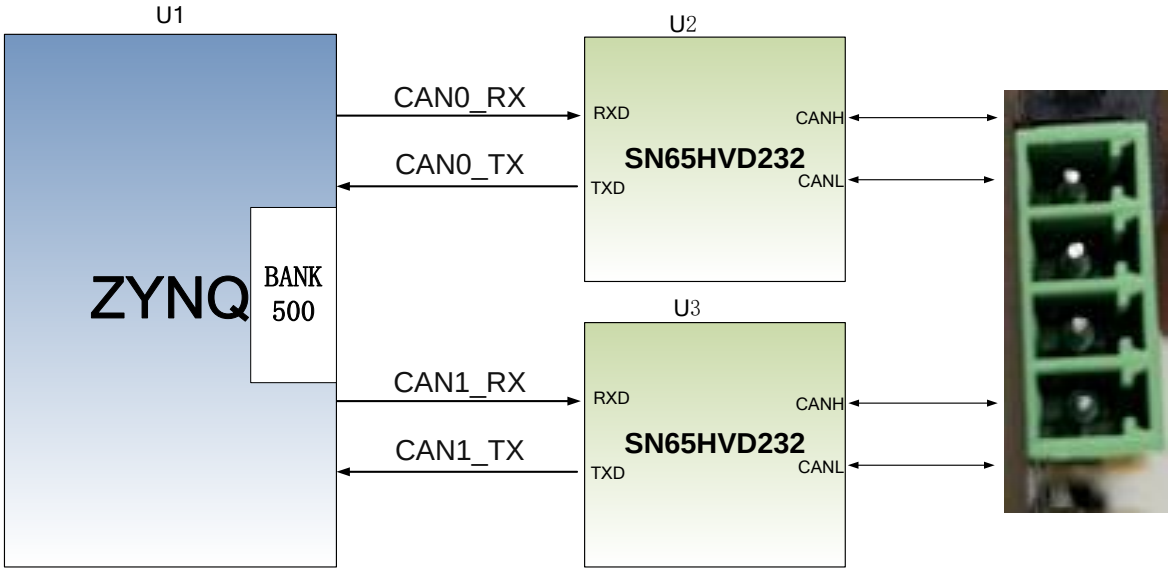


Figure 3-2-1 Connection diagram of CAN transceiver chip on PS side

CAN communication pin assignment:

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number	Description
CAN0_RX	PS_MIO10	E9	CAN0 Receiver
CAN0_TX	PS_MIO11	C6	CAN0 Transmitter
CAN1_RX	PS_MIO13	E8	CAN1 Receiver
CAN1_TX	PS_MIO12	D9	CAN1 Transmitter

3.3 485 Communication Interface

There are two 485 communication interfaces on the AX7Z020B carrier board. Among them, 485 communication interface 1 is connected to the GPIO interface of BANK500 on the PS system, and 485 communication interface 2 is connected to the

GPIO interface of BANK34 on the PL system. The 485 transceiver chip is the MAX3485 chip from MAXIM for the user's 485 communication service.

Figure 3-3-1 shows the connection diagram of the 485 transceiver chip on the PL side:

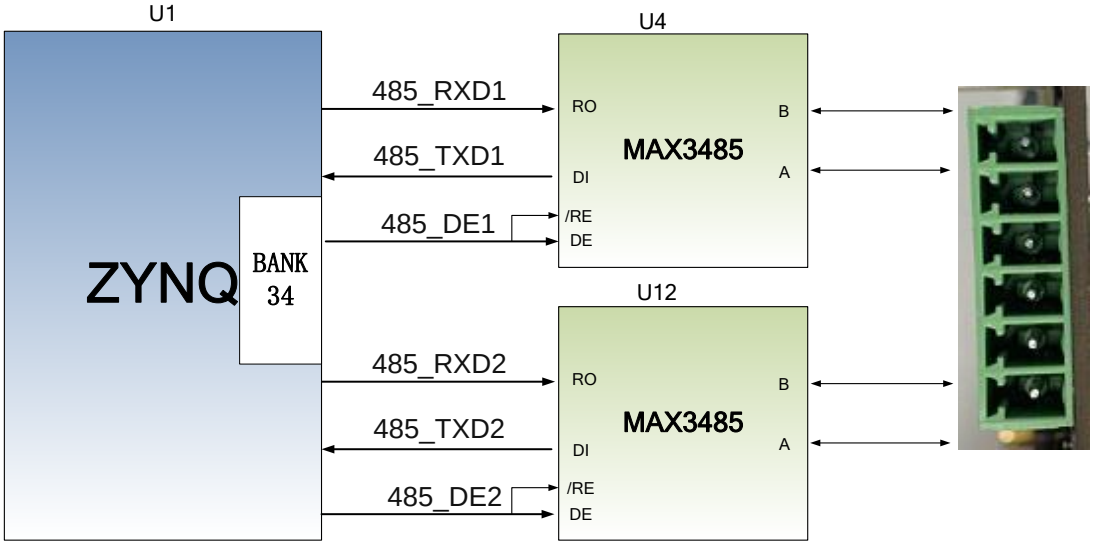


Figure 3-3-1 Connection diagram of RS485chip and interface

485 communication pin assignment:

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number	Description
485_TXD1	PS_MIO15	C8	485 Transmitter 1
485_RXD1	PS_MIO14	C5	485 Receiver 1
485_DE1	PS_MIO9	B5	485 Receive launch enable1
485_TXD2	IO34_L4N	W13	485 Transmitter 2
485_RXD2	IO34_L4P	V12	485 Receiver 2
485_DE2	IO34_L12N	U19	485 Receive launch enable 2

3.4 Gigabit Ethernet Interface

The AX7Z020B carrier board has 1 Gigabit Ethernet interface, which is connected to the GPIO interface of BANK501 on the PS system side. The Ethernet chip adopts JL Semiconductor's industrial grade Ethernet GPHY chip (JL2121-N040I) to provide users with network communication services. The Ethernet PHY chip on the PS side is connected to the MIO interface of the BANK502 on the PS on ZYNQ, while it on the PL side is connected to the IO of BANK66.

The JL2121 chip supports 10/100/1000 Mbps network transmission rate, and

performs data communication with the MAC layer of the MPSOC system through the RGMII interface. JL2121D supports MDI/MDX self-adaptive, various speeds self-adaptive, Master/Slave self-adaptive, and supports MDIO bus for PHY register management.

When the JL2121 is powered on, it will detect the level status of some specific IOs to determine its own operating mode. Figure 3-4-1 describes the default settings after the GPHY chip is powered on.

Configuration Pin	Description	Configuration Value
RXD3_ADR0 RXC_ADR1 RXCTL_ADR2	PHY address in MDIO/MDC mode	PHY Address is 001
RXD1_TXDLY	TX clock 2ns delay	Delay
RXD0_RXDLY	RX clock 2ns delay	Delay

Figure 3-4-1 GPHY chip default configuration values

When the network is connected to Gigabit Ethernet, the data transmission of ZYNQ and PHY chip JL2121 is communicated through the RGMII bus, the transmission clock is 125Mhz, and the data is sampled on the rising edge and falling edge of the clock.

When the network is connected to 100M Ethernet, the data transmission of ZYNQ and PHY chip JL2121 is communicated through RMII bus, and the transmission clock is 25Mhz. Data is sampled on the rising edge and falling edge of the clock.

Figure 3-4-1 shows the connection diagram of 1-channel Ethernet PHY chip on ZYNQ PS side:

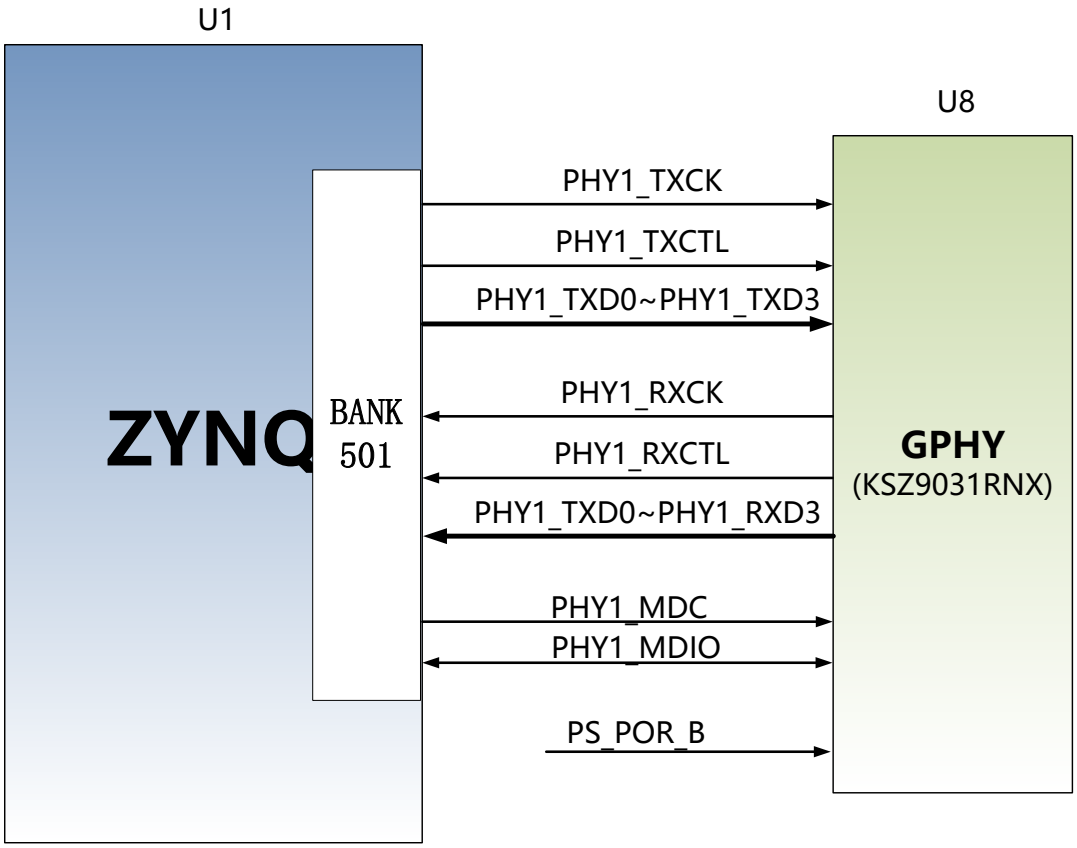


Figure 3-4-1 Connection diagram between ZYNQ PS system and GPHY

Gigabit Ethernet pin assignment:

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number	Description
ETH_TXCK	PS_MIO16	A19	RGMII sends the clock
ETH_TXD0	PS_MIO17	E14	Send data bit0
ETH_TXD1	PS_MIO18	B18	Send data bit1
ETH_TXD2	PS_MIO19	D10	Send data bit2
ETH_TXD3	PS_MIO20	A17	Send data bit3
ETH_TXCTL	PS_MIO21	F14	Send the enable signal
ETH_RXCK	PS_MIO22	B17	RGMII receives the clock
ETH_RXD0	PS_MIO23	D11	Receive data Bit0
ETH_RXD1	PS_MIO24	A16	Receive data Bit1
ETH_RXD2	PS_MIO25	F15	Receive data Bit2
ETH_RXD3	PS_MIO26	A15	Receive data Bit3
ETH_RXCTL	PS_MIO27	D13	Receive data valid signal

ETH_MDC	PS_MIO52	C10	MDIO manages the clock
ETH_MDIO	PS_MIO53	C11	MDIO manages data
PS_POR_B	PS_POR_B	C7	Reset signal

3.5 USB2.0 Host Interface

The AX7Z020B carrier board has a USB2.0 HOST interface. The USB2.0 transceiver uses a 1.8V, high-speed USB3320C-EZK chip that supports the ULPI standard interface. The USB bus interface of ZYNQ is connected to the USB3320C-EZK transceiver to realize high-speed data communication in USB2.0 Host mode. The USB data and control signals of the USB3320C are connected to the IO port of the BANK501 on the PS side of the ZYNQ chip. The 24MHz crystal oscillator provides the system clock for the USB3320C chip.

The USB interface is a flat USB interface (USB Type A), which is convenient for users to connect different USB Slave peripherals (such as USB mouse and USB keyboard) at the same time. In addition, the carrier board provides a +5V power supply for the USB interface.

The connection diagram between the ZYNQ processor and the USB3320C-EZK chip is shown in 3-5-1:

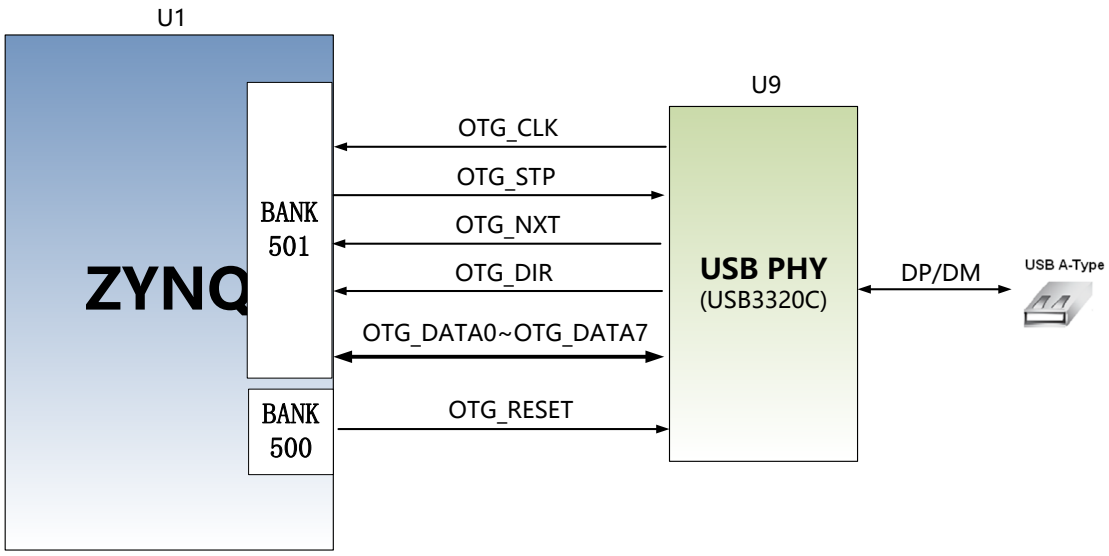


Figure 3-5-1 Connection diagram between Zynq7000 and USB chip

USB2.0 pin assignment:

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number	Description
OTG_DATA4	PS_MIO28	C16	USB data Bit4
OTG_DIR	PS_MIO29	C13	USB data direction signal
OTG_STP	PS_MIO30	C15	USB stop signal
OTG_NXT	PS_MIO31	E16	USB next data signal
OTG_DATA0	PS_MIO32	A14	USB data Bit0
OTG_DATA1	PS_MIO33	D15	USB data Bit1
OTG_DATA2	PS_MIO34	A12	USB data Bit2
OTG_DATA3	PS_MIO35	F12	USB data Bit3
OTG_CLK	PS_MIO36	A11	USB clock signal
OTG_DATA5	PS_MIO37	A10	USB data Bit5
OTG_DATA6	PS_MIO38	E13	USB data Bit6
OTG_DATA7	PS_MIO39	C18	USB data Bit7
OTG_RESETN	PS_MIO46	D16	USB reset signal

3.6 USB to Serial Port

The AX7Z020B carrier board is equipped with a USB-to-UART interface for the overall debugging of ZYNQ7000 system. The conversion chip is USB-UAR chip of Silicon Labs CP2102GM, and the USB interface is MINI USB, which can be connected to the USB port of PC with a USB cable for separate power supply of the core board and serial data communication.

Figure 3-6-1 shows the schematic diagram of USB Uart circuit design:

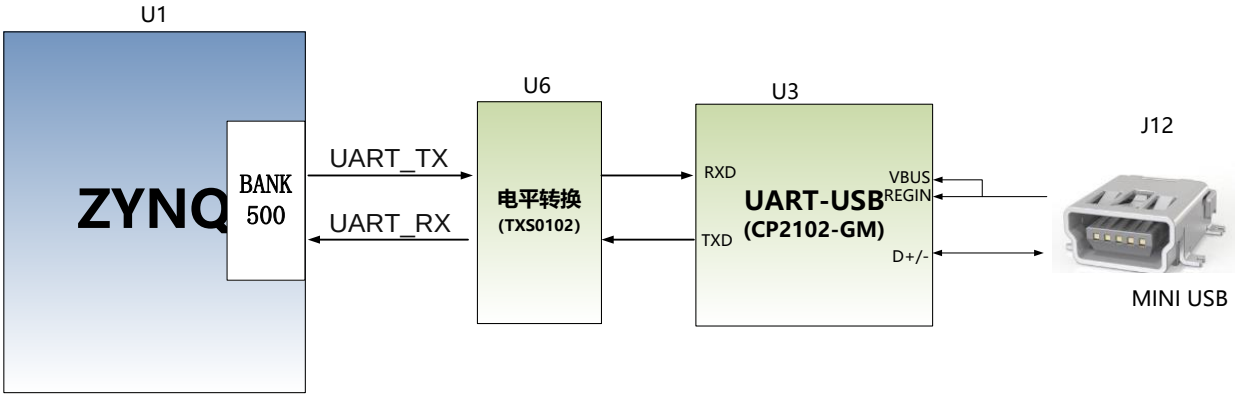


Figure 3-6-1 Schematic diagram of USB to serial port

ZYNQ pin assignment of UART to serial port:

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number	Description
UART_RX	PS_MIO49	C12	Uart data input
UART_TX	PS_MIO48	B12	Uart data output

3.7 AD Input Interface

The AX7Z020B carrier board is equipped with four AD input interfaces, two of which are used to collect external analog signals for AD conversion, and the other two are used to measure the power supply voltage and current of the development board. Two analog signals used to collect the external analog signals for AD conversion uses the SMA connector as the input, converts input signals into differential signals, and then inputs them into ZYNQ. Power current measurement is connected to VP and VN (ZYNQ's dedicated AD input pins).

Figure 3-7-1 shows the schematic diagram of AD acquisition circuit design:

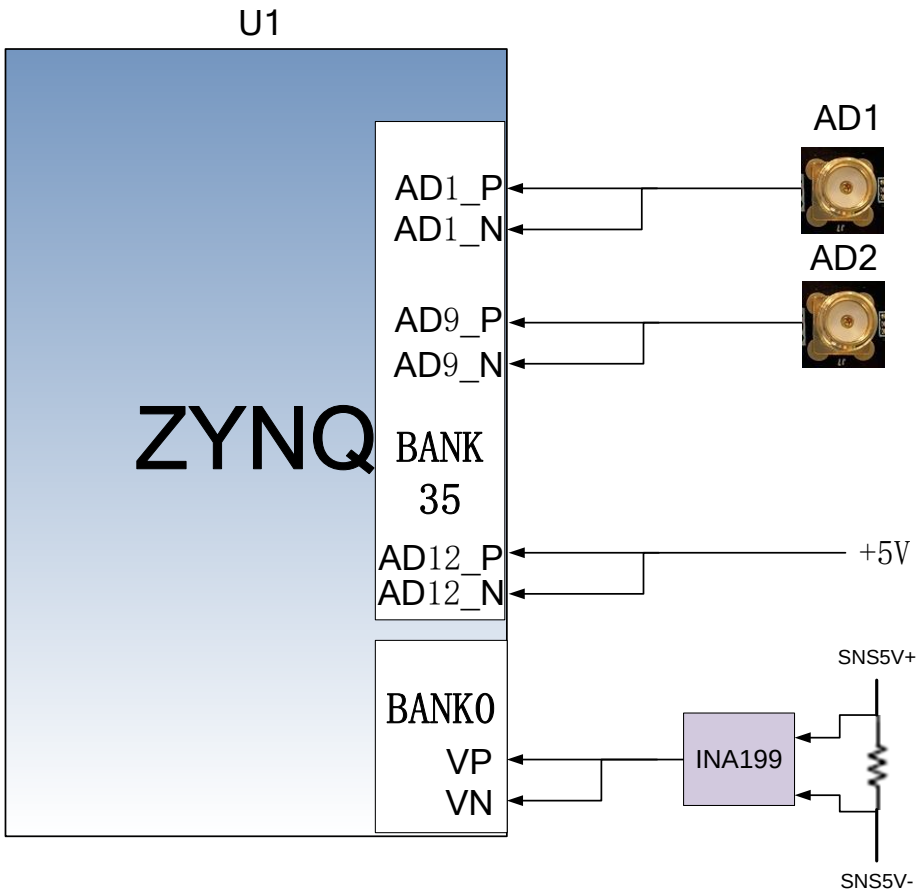


Figure 3-7-1 Circuit design of AD acquisition

ZYNQ pin assignment of AD acquisition circuit:

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number	Description
XADC_AD1P	IO35_L3P	E17	AD_IN_P
XADC_AD1N	IO35_L3N	D18	AD_IN_N
XADC_AD9P	IO35_L5P	E18	AD_IN_P
XADC_AD9N	IO35_L5N	E19	AD_IN_N
XADC_AD12P	IO35_L15P	F19	AD_IN_P
XADC_AD12N	IO35_L15N	F20	AD_IN_N
VP	VP	K9	AD_IN_P
VN	VN	L10	AD_IN_N

3.8 HDMI Output Interface

HDMI, the full name is High Definition Multimedia Interface. The AX7Z020B development board directly connects to the differential signal and clock of the HDMI interface through the differential IO of ZYNQ, implementing the differential to parallel conversion and codecing of HMDI signals inside ZYNQ, and implementing the transmission solution of DMI digital video input and output, which supports a maximum of 1080P@60Hz input and output.

The HDMI signal is connected to the BANK34 of the PL side of ZYNQ, the design schematic is shown in Figure 3-8-1 below:

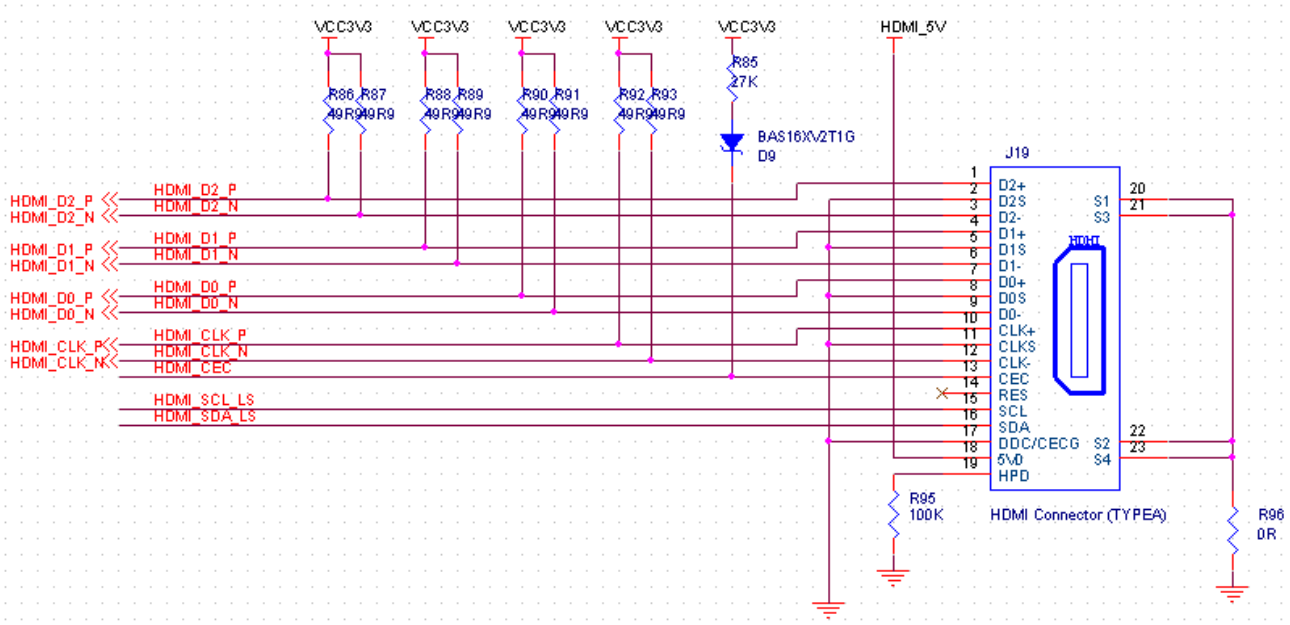


Figure 3-8-1 Design schematic of HDMI interface

ZYNQ pin assignment:

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number	Description
HDMI_CLK_P	IO34_L3P	U13	HDMI clock signal, positive
HDMI_CLK_N	IO34_L3N	V13	HDMI clock signal, negative
HDMI_D0_P	IO34_L8P	W14	HDMI data 0 positive
HDMI_D0_N	IO34_L8N	Y14	HDMI data 0 negative
HDMI_D1_P	IO34_L17P	Y18	HDMI data 1 positive
HDMI_D1_N	IO34_L17N	Y19	HDMI data 1 negative
HDMI_D2_P	IO34_L7P	Y16	HDMI data 2 positive

HDMI_D2_N	IO34_L7N	Y17	HDMI data 2 negative
HDMI_SCL	IO34_L21N	V18	HDMI IIC clock
HDMI_SDA	IO34_L21P	V17	HDMI IIC data

3.9 MIPI Camera Interface (Only for AX7Z020B)

The AX7Z020B carrier board has a MIPI camera interface, which can be used to connect to ALINX MIPI OV5640 camera module. Figure 3-9-1 shows the circuit schematic diagram of the MIPI interface:

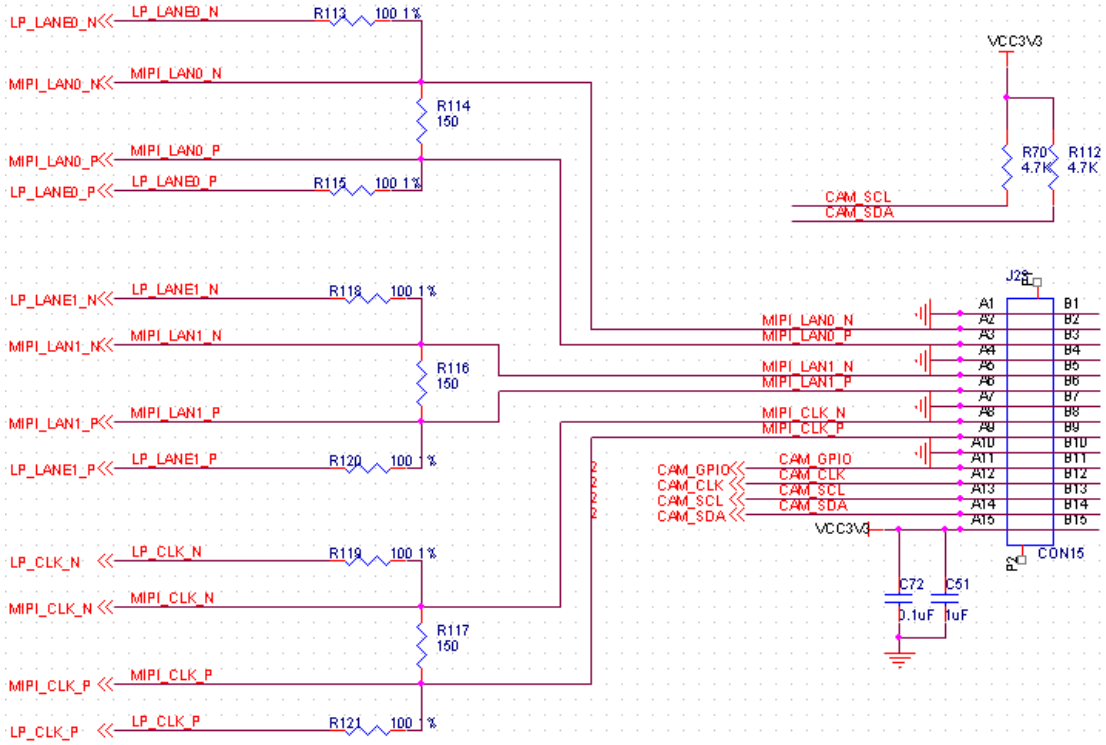


Figure 3-9-1 Design schematic of HDMI interface

MIPI interface pin assignment:

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number	Description
LP_CLK_P	IO13_L15P	V8	Low Power mode's clock, positive
LP_CLK_N	IO13_L15N	W8	Low Power mode's clock, negative
LP_LANE0_P	IO13_L12P	T9	Low Power mode's LANE0, positive

LP_LANE0_N	IO13_L12N	U10	Low Power mode's LANE0, negative
LP_LANE1_P	IO13_L20P	Y12	Low Power mode's LANE1, positive
LP_LANE1_N	IO13_L20N	Y13	Low Power mode's LANE1, negative
MIPI_CLK_P	IO13_L13P	Y7	High Speed mode's clock, positive
MIPI_CLK_N	IO13_L13N	Y6	High Speed mode's clock, negative
MIPI_LAN0_P	IO13_L18P	W11	High Speed mode's LANE0, positive
MIPI_LAN0_N	IO13_L18N	Y11	High Speed mode's LANE0, negative
MIPI_LAN1_P	IO13_L17P	U9	High Speed mode's LANE1, positive
MIPI_LAN1_N	IO13_L17N	U8	High Speed mode's LANE1, negative
CAM_GPIO	IO13_L11P	U7	GPIO control of camera
CAM_CLK	IO13_L11N	V7	Clock input of camera
CAM_SCL	IO13_L19P	T5	I2C clock of camera
CAM_SDA	IO13_L19N	U5	I2C data of camera

3.10 SD Card Slot

The AX7Z020B carrier board has a Micro-type SD card interface to provide user access to the SD card memory for storing ZYNQ chip BOOT programs, Linux operating system kernel, file system, and other user data files.

The SDIO signal is connected to the IO signal of ZYNQ's PS BANK501, because the BANK's VCCMIO is set to 1.8V, but the SD card's data level is 3.3V, so we use TXS02612 level converter to connect them. The Zynq7000 PS and SD card connectors are shown in Figure 3-10-1.

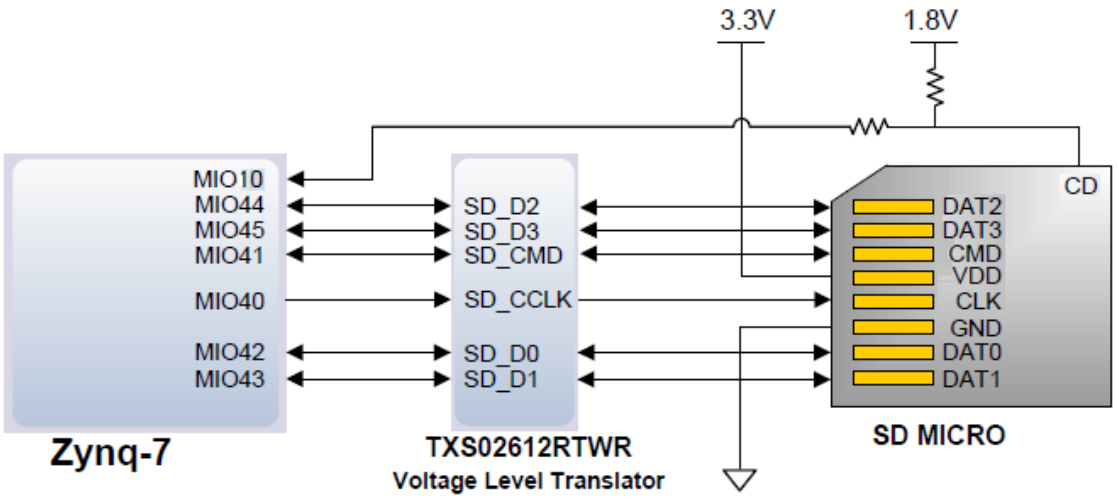


Figure 3-10-1 connection diagram of SD card

SD card slot pin assignment:

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number	Description
SD_CLK	PS_MIO40	D14	SD clock signal
SD_CMD	PS_MIO41	C17	SD command signal
SD_D0	PS_MIO42	E12	SD data Data0
SD_D1	PS_MIO43	A9	SD data Data1
SD_D2	PS_MIO44	F13	SD data Data2
SD_D3	PS_MIO45	B15	SD Data Data3
SD_CD	PS_MIO47	B14	SD card insertion signal

3.11 EEPROM

The AX7Z020B development board has an EEPROM onboard.The model of the EEPROM is 24LC04, and the capacity is 4Kbit (2 * 256 * 8bit), which is composed of two 256byte blocks and communicates through the IIC bus. The on-board EEPROM is set to learn the communication method of IIC bus. The I2C signal of EEPROM is connected to the I2C interface of the ZYNQ PS side. Figure 3-11-1 shows the connection diagram of EEPROM:

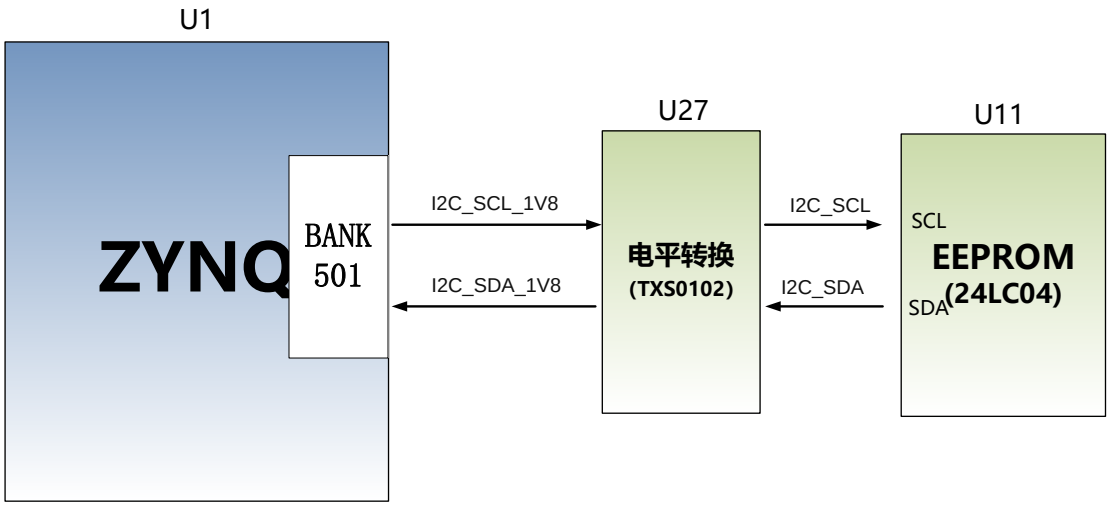


Figure 3-11-1 EEPROM connection diagram

EEPROM pin assignment:

Signal Name	ZYNQ Pin Name	ZYNQ Pin No.	Description
I2C_SCL_1V8	MIO50	B13	IIC Clock Signal
I2C_SDA_1V8	MIO51	B9	IIC Data Signal

3.12 Real-time Clock

The FPGA development board has a real-time clock RTC chip, model DS1338, which can provide the calendar until 2099, including year, month, day, minute, second, and week. If time is needed in the system, then RTC needs to be involved in the product, and it needed to externally connect a 32.768KHz passive clock to provide accurate clock source to the clock chip, so that RTC can accurately provide clock information to the product. At the same time, in order for the real-time clock to run normally after the product is powered off, an additional battery is usually required to power the clock chip. After we put the button cell (model CR1220, voltage is 3V) into the system, when the system loses the battery, the button cell can also supply power to DS1338. In this way, no matter whether the product is powered or not, DS1338 will operate normally without interruption and can provide continuous time information. The interface signals of the RTC and EEPORM share the same I2C bus. Figure 3-12-1 shows the connection diagram of DS1338.

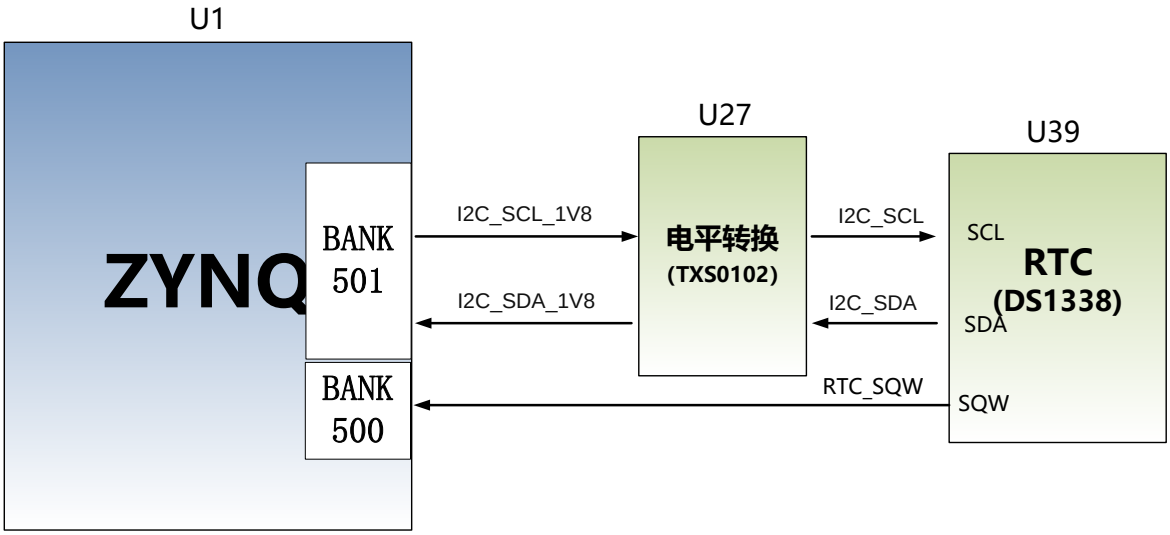


Figure 3-12-1 DS1338 schematic diagram

DS1338 interface pin assignment:

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number	Description
I2C_SCL_1V8	MIO50	B13	RTC Clock Signal
I2C_SDA_1V8	MIO51	B9	RTC reset signal
RTC_SQW	MIO7	D8	Square wave output signal

3.13 Temperature Sensor

A high-precision, low-power, digital temperature sensor chip is installed on the AX7Z020B development board, and the model is LM75 from ON Semiconductor company. The temperature accuracy of the LM75 chip is 0.5 degrees, and the sensor and FPGA are I2C digital interfaces. ZYNQ7020 reads the temperature near the current development board through the I2C interface. The interface signal of the LM75 sensor and EEPORM share the same I2C bus. Figure 3-13-1 below shows the connection diagram of the LM75 sensor.

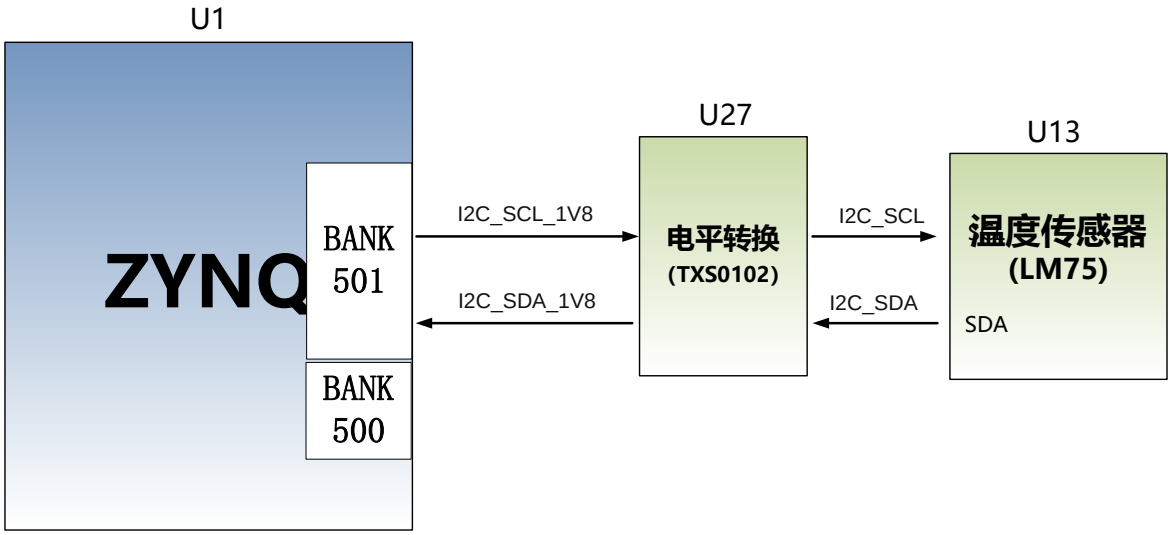


Figure 3-13-1 Connection diagram of LM75 sensor

3.14 JTAG Interface

The downloading and debugging circuit of JTAG is reserved on the carrier board of AX7Z020B to extract the JTAG debugging signals (TCK,TDO,TMS, TDI) of ZYNQ. Figure 3-14-1 shows the schematic diagram of the JTAG interface on the development board:

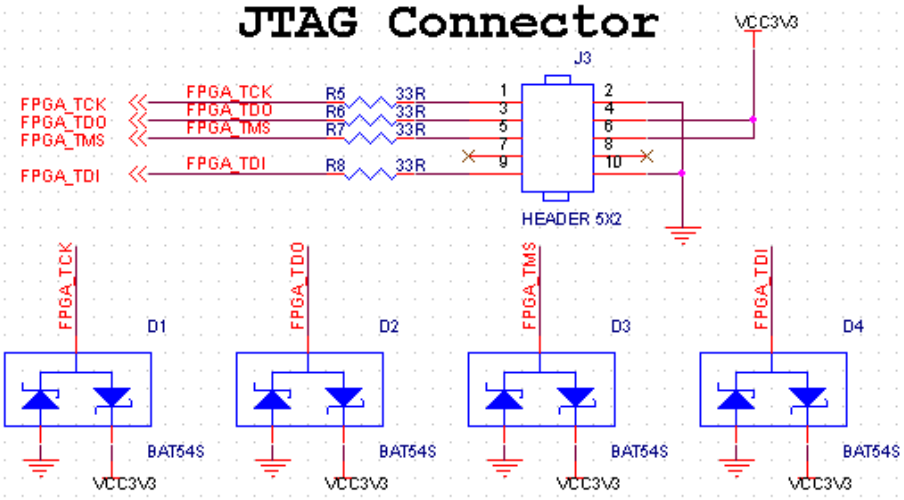


Figure 3-14-1 Schematic diagram of JTAG Interface

3.15 User LEDs

There are four user LED lights (LED1~LED4) on the AX7Z020B carrier board. All four user LED lights are connected to the IO of the BANK35 on the PL side, and users can control the on and off through the program. When the connected IO voltage of the user LED light is high, the user LED light will off, and when the connected IO voltage is low, the user LED will light up. Figure 3-15-1 shows the connection diagram of LED hardware:

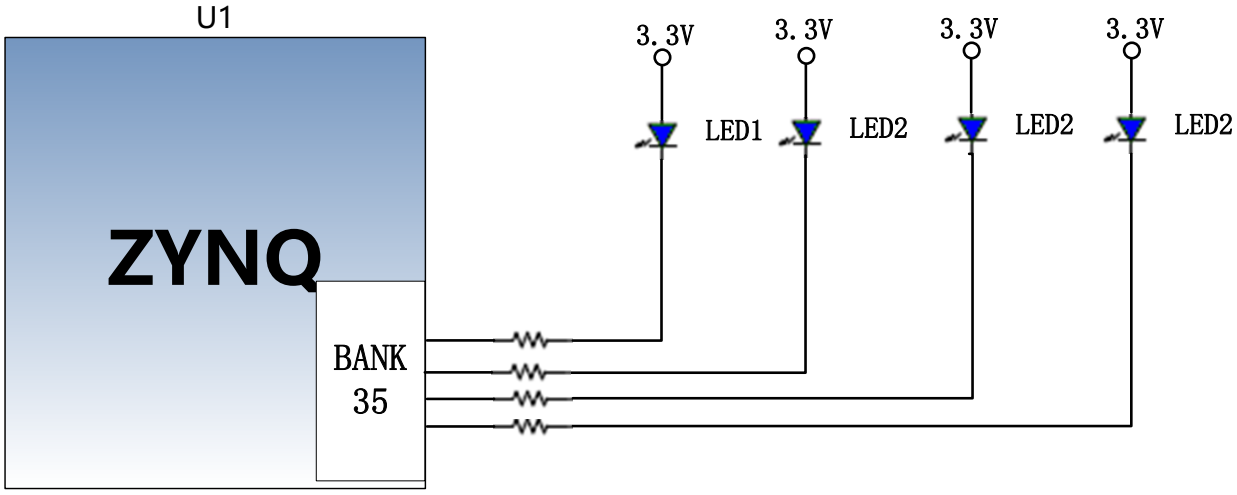


Figure 3-15-1 Connection diagram of LEDs hardware

Pin assignment of user LEDs:

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number	Description
LED1	IO35_L20N	J14	User LED1
LED2	IO35_L20P	K14	User LED2
LED3	IO35_L14P	J18	User LED3
LED4	IO35_L14N	H18	User LED4

3.16 User Keys

There are 4 user keys (KEY1 ~ KEY4) on the AX7Z020B carrier board, and the 4 user keys are connected to the IO of the BANK35 on the PL side. When the button is pressed, indicating the signal is low. The ZYNQ chip will detect whether it has the low level to determine whether the button is pressed. Figure 3-16-1 shows the diagram of

user key connection:

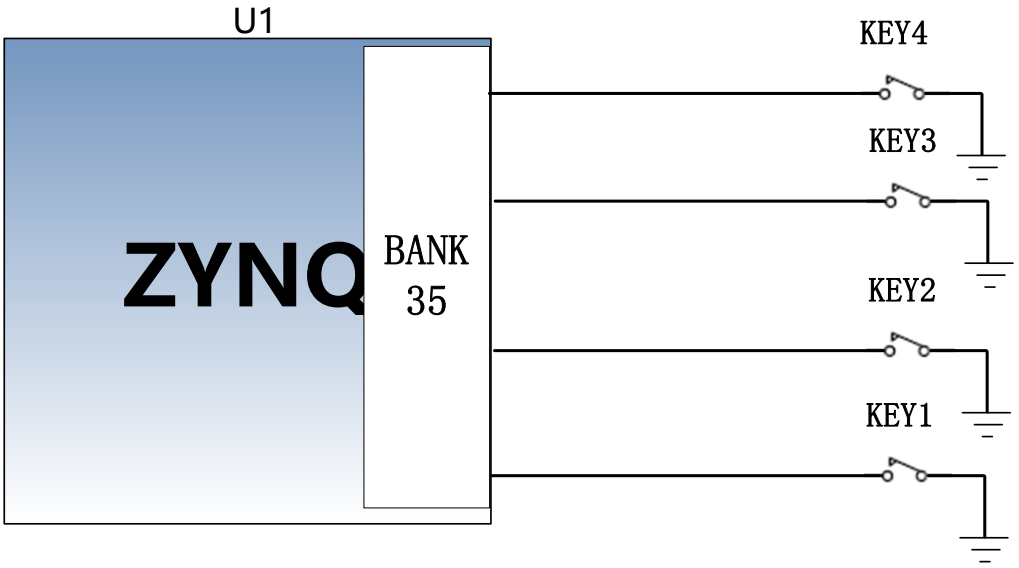


Figure 3-16-1 Connection diagram of user keys

ZYNQ pin assignment of user keys:

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number	Description
KEY1	IO35_L23N	M15	User KEY1
KEY2	IO35_L23P	M14	User KEY2
KEY3	IO35_L11N	L17	User KEY3
KEY4	IO35_L11P	L16	User KEY4

3.17 Expansion Port

The carrier board is reserved with two 0.1-inch standard pitch 40-pin expansion ports J20 and J21, which are used to connect the ALINX modules or the external circuit designed by the user himself. The expansion port has 40 signals: one 5V power supply, two 3.3 V power supplies, 3 ground supplies and 34 IOs. **Do not connect the IO directly to the 5V device to avoid burning the FPGA ZYNQ7000 chip. If you want to connect a 5V device, you need to connect a level conversion chip.**

Figure 3-17-1 shows the circuit of the expansion port (J20):

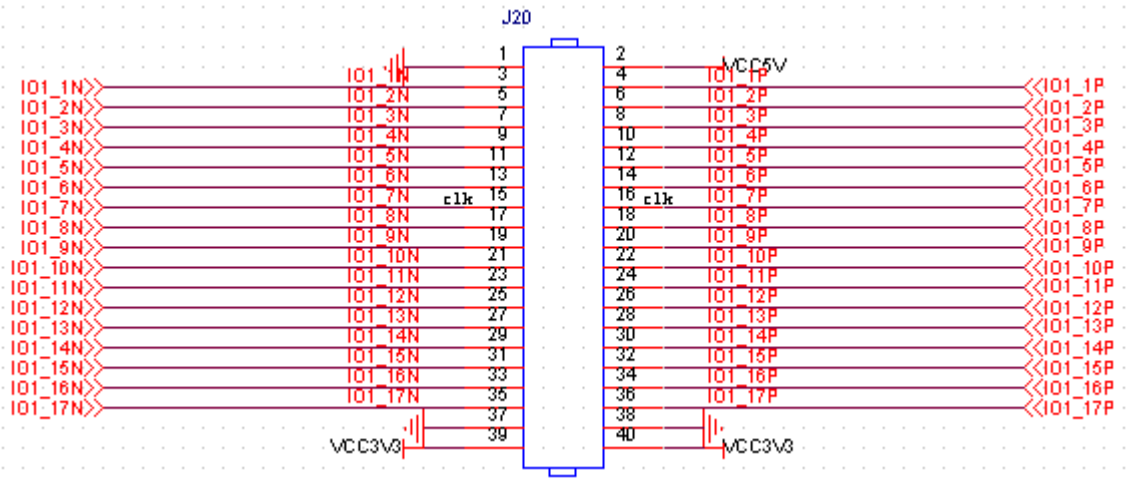


Figure 3-17-1 Schematic diagram of J20

Pin assignment of J20 expansion port:

Pin No.	ZYNQ Pin	Pin No.	ZYNQ Pin
1	GND	**2**	+5V
3	R14	**4**	P14
5	U12	**6**	T12
7	T15	**8**	T14
9	T11	**10**	T10
11	U15	**12**	U14
13	P19	**14**	N18
15	R17	**16**	R16
17	P15	**18**	P16
19	N17	**20**	P18
21	V16	**22**	W16
23	R18	**24**	T17
25	W19	**26**	W18
27	W20	**28**	V20
29	P20	**30**	N20
31	U17	**32**	T16
33	U20	**34**	T20
35	V15	**36**	W15
37	GND	**38**	GND
39	+3.3V	**40**	+3.3V

Figure 3-17-2 shows the circuit of the expansion port (J21):

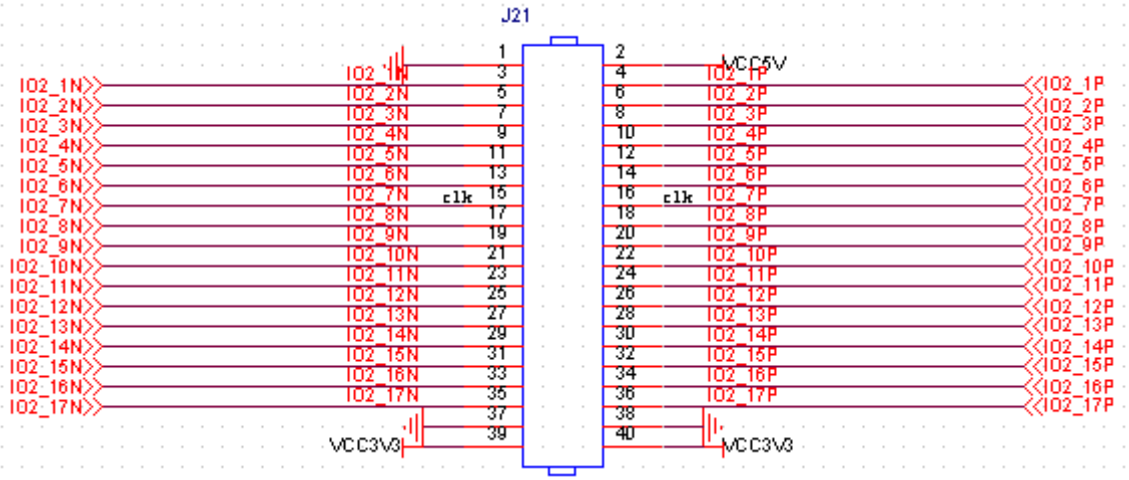


Figure 3-17-2 Schematic diagram of J21

Pin assignment of J21 expansion port:

Pin No.	ZYNQ Pin	Pin No.	ZYNQ Pin
1	GND	**2**	+5V
3	M18	**4**	M17
5	K19	**6**	J19
7	B19	**8**	A20
9	B20	**10**	C20
11	G19	**12**	G20
13	M19	**14**	M20
15	D20	**16**	D19
17	L20	**18**	L19
19	F16	**20**	F17
21	H20	**22**	J20
23	G18	**24**	G17
25	H17	**26**	H16
27	G15	**28**	H15
29	K18	**30**	K17
31	J16	**32**	K16
33	N16	**34**	N15
35	L15	**36**	L14
37	GND	**38**	GND

39	+3.3V	**40**	+3.3V

3.18 Power Supply

The power input voltage of the AX7Z020B FPGA development board is DC5V, please use the power supply equipped on the development board, do not use other power supplies, so as to avoid damaging the development board. On the carrier board, two DC / DC power chips ETA1471 and one LDO power chip SPX3819M5-ADJ are converted into three power supplies: 1.8V, + 3.3V and VCCIO35.

The IO level of the BANK35 on ZYNQ7020 can be adjusted by the jumper cap on the carrier board. By default, if no jumper cap is installed on J28 and J29, the IO level of the BANK35 is 3.3V. If the J29 has a jumper cap installed, the IO level of the BANK35 is 1.8V. If the J28 has a jumper cap installed, the IO level of the BANK35 is 2.5V.

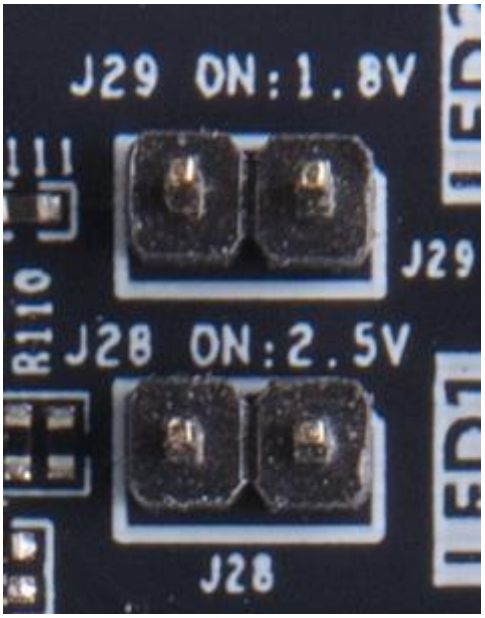
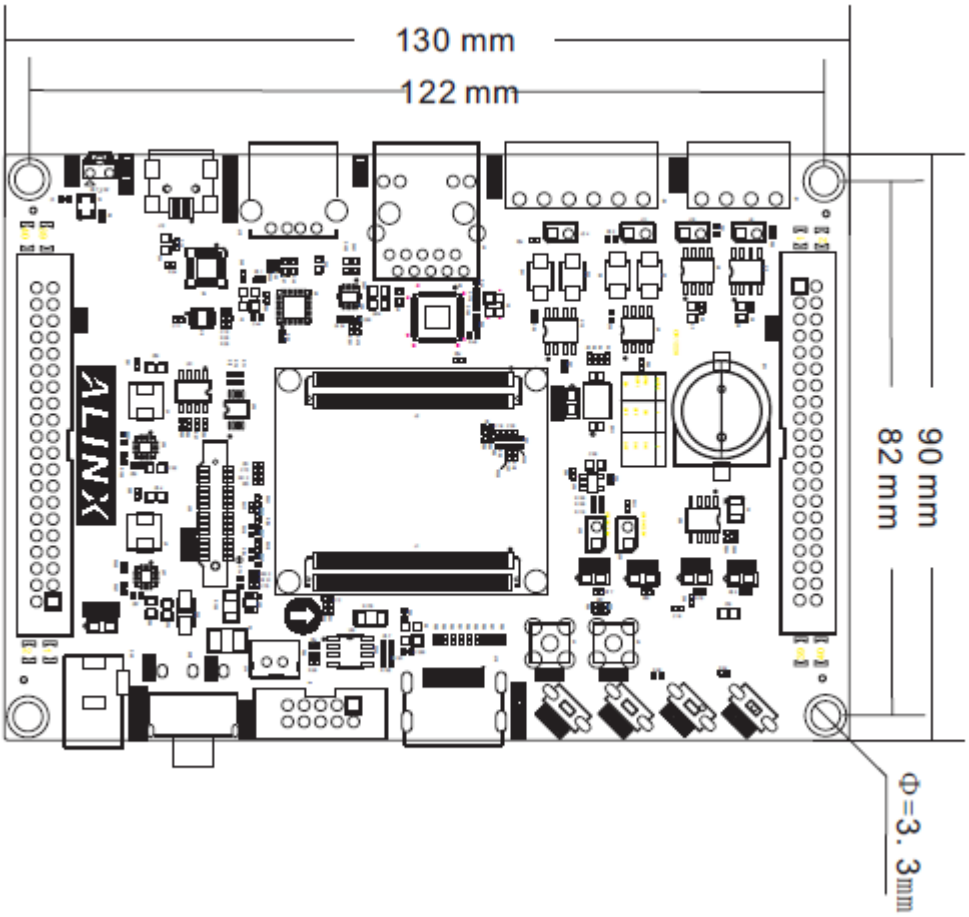


Figure 3-18-1 VCCIO35 voltage adjustment

3.19 Size Dimension of Carrier Board



Top View