

DEPG0154RWS800F6

Specification for 1.54 inch EPD

Model NO. : DEPG0154RWS800F6

Confirmation:

Prepared by	Checked by	Approved by

Customer approval:

Customer	Approved by	Date

Revision History

Version	Content	Date	Producer
1.0	New release	2019/06/10	
1.1	Update Mechanical Drawing of EPD Module	2019/11/05	

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1. Over View

DEPG0154RWS800F6 is an Active Matrix Electrochromic Display (AM EPD), with interface and a reference system design. The display is capable to display images at 1-bit white, black and red full display capabilities. The 1.54inch active area contains 152×152 pixels. The module is a TFT-array driving electrophoresis display, with integrated circuits including gate driver, source driver, MCU interface, timing controller, oscillator, DC-DC, SRAM, LUT, VCOM. Module can be used in portable electronic devices, such as Electronic Shelf Label (ESL) System.

2. Features

- ◆ 152×152 pixels display
- ◆ High contrast High reflectance
- ◆ Ultra wide viewing angle Ultra low power consumption
- ◆ Pure reflective mode
- ◆ Bi-stable display
- ◆ Commercial temperature range
- ◆ Landscape portrait modes
- ◆ Hard-coat antiglare display surface
- ◆ Ultra Low current deep sleep mode
- ◆ On chip display RAM
- ◆ Waveform can stored in On-chip OTP or written by MCU
- ◆ Serial peripheral interface available
- ◆ On-chip oscillator
- ◆ On-chip booster and regulator control for generating VCOM, Gate and Source driving voltage
- ◆ I²C signal master interface to read external temperature sensor
- ◆ Built-in temperature sensor

3. Mechanical Specification

Parameter	Specifications	Unit	Remark
Screen Size	1.54	Inch	
Display Resolution	152(H)×152(V)	Pixel	DPI:140
Active Area	27.512×27.512	mm	
Pixel Pitch	0.181×0.181	mm	
Pixel Configuration	Square		
Outline Dimension	31.8(H)×37.32 (V) ×1.0 (D)	mm	
Weight	2.18±0.5	g	

4.Mechanical Drawing of EPD Module

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FRONT VIEW

SIDE VIEW

BACK VIEW

Pixel Pitch

NOTE

- 1 DISPLAY MODULE 1.54" ARRAY FOR EPD
- 2 DRIVER IC:SSD1680Z8
- 3 RESOLUTION:152gateX152source
- 4 PIXEL SIZE: 0.181mmX 0.181 mm

TOLERANCES UNMARKED ANGLES±5° .X=±0.4mm .XX=±0.20mm .XXX=±0.200mm	TITLE: EPD DWN. XZ FAN	PROJECT: DEPG0154_F6 CHK. PP SUN	REV.: A UNIT: mm	DATE: 19.08.06 3RD ANGLE: 	CUST. P/N: PAGE: 1/1
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5. Input/output Pin Assignment

No.	Name	I/O	Description	Remark
1	NC		Do not connect with other NC pins	Keep Open
2	GDR	O	N-Channel MOSFET Gate Drive Control	
3	RESE	I	Current Sense Input for the Control Loop	
4	NC	NC	Do not connect with other NC pins	Keep Open
5	VSH2	C	Positive Source driving voltage(Red)	
6	TSCL	O	I2C Interface to digital temperature sensor Clock pin	
7	TSDA	I/O	I2C Interface to digital temperature sensor Data pin	
8	BS1	I	Bus Interface selection pin	Note 5-5
9	BUSY	O	Busy state output pin	Note 5-4
10	RES#	I	Reset signal input. Active Low.	Note 5-3
11	D/C#	I	Data /Command control pin	Note 5-2
12	CS#	I	Chip select input pin	Note 5-1
13	SCL	I	Serial Clock pin (SPI)	
14	SDA	I/O	Serial Data pin (SPI)	
15	VDDIO	P	Power Supply for interface logic pins It should be connected with VCI	
16	VCI	P	Power Supply for the chip	
17	VSS	P	Ground	
18	VDD	C	Core logic power pin VDD can be regulated internally from VCI. A capacitor should be connected between VDD and VSS	
19	VPP	P	FOR TEST	Keep Open
20	VSH1	C	Positive Source driving voltage	
21	VGH	C	Power Supply pin for Positive Gate driving voltage and VSH1	
22	VSL	C	Negative Source driving voltage	
23	VGL	C	Power Supply pin for Negative Gate driving voltage VCOM and VSL	
24	VCOM	C	VCOM driving voltage	

I = Input Pin, O =Output Pin, I/O = Bi-directional Pin (Input/output), P = Power Pin, C = Capacitor Pin

Note 5-1: This pin (CS#) is the chip select input connecting to the MCU. The chip is enabled for MCU

communication only when CS# is pulled LOW.

Note 5-2: This pin is (D/C#) Data/Command control pin connecting to the MCU in 4-wire SPI mode. When the pin is pulled HIGH, the data at SDA will be interpreted as data. When the pin is pulled LOW, the data at SDA will be interpreted as command.

Note 5-3: This pin (RES#) is reset signal input. The Reset is active low.

Note 5-4: This pin is Busy state output pin. When Busy is High, the operation of chip should not be interrupted, command should not be sent. The chip would put Busy pin High when -Outputting display waveform -Communicating with digital temperature sensor

Note 5-5: Bus interface selection pin

BS1 State	MCU Interface
L	4-lines serial peripheral interface(SPI) - 8 bits SPI
H	3- lines serial peripheral interface(SPI) - 9 bits SPI

6. Electrical Characteristics

6.1 Absolute Maximum Rating

Parameter	Symbol	Rating	Unit
Logic supply voltage	VCI	-0.5 to +4.0	V
Logic Input voltage	VIN	-0.5 to VCI +0.5	V
Logic Output voltage	VOUT	-0.5 to VCI +0.5	V
Operating Temp range	TOPR	0 to +40	°C.
Storage Temp range	TSTG	-25 to+40	°C.
Optimal Storage Temp	TSTGo	23±2	°C.
Optimal Storage Humidity	HSTGo	55±10	%RH

Note:

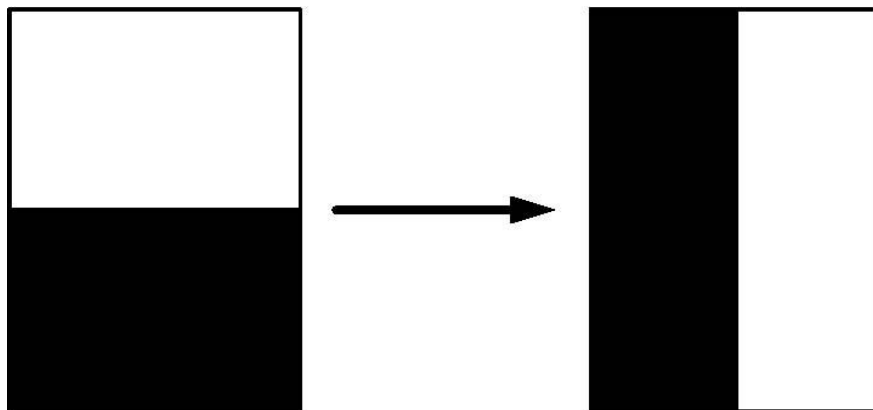
1.Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Panel DC Characteristics tables.

6.2 Panel DC Characteristics

The following specifications apply for: VSS=0V, VCI=3.0V, TOPR =23°C.

Parameter	Symbol	Condition	Applicable pin	Min.	Typ.	Max.	Unit
Single ground	V _{SS}	-		-	0	-	V
Logic supply voltage	V _{CI}	-	V _{CI}	2.2	3.0	3.7	V
Core logic voltage	V _{DD}		V _{DD}	1.7	1.8	1.9	V
High level input voltage	V _{IH}	-	-	0.8 V _{CI}	-	-	V
Low level input voltage	V _{IL}	-	-	-	-	0.2 V _{CI}	V
High level output voltage	V _{OH}	I _{OH} = -100uA	-	0.9 V _{CI}	-	-	V
Low level output voltage	V _{OL}	I _{OL} = 100uA	-	-	-	0.1 V _{CI}	V
Typical power	P _{TYP}	V _{CI} =3.0V	-	-	8.4	-	mW
Deep sleep mode	P _{STPY}	V _{CI} =3.0V	-	-	0.003	-	mW
Typical operating current	I _{opr_VCI}	V _{CI} =3.0V	-	-	2.8	-	mA
Image update time	-	23 °C	-	-	14	-	sec
Sleep mode current	I _{slp_VCI}	DC/DC off No clock No input load Ram data retain	-	-	20		uA
Deep sleep mode current	I _{dslp_VCI}	DC/DC off No clock No input load Ram data not retain	-	-	1	5	uA

Notes: 1. The typical power is measured with following transition from horizontal 2 scale pattern to vertical 2 scale pattern.



2. The deep sleep power is the consumed power when the panel controller is in deep sleep mode.
3. The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by Maker .

6.3 Panel DC Characteristics(Driver IC Internal Regulators)

The following specifications apply for: VSS=0V, VCI=3.0V, TOPR =23°C.

Parameter	Symbol	Condition	Applicable pin	Min.	Typ.	Max.	Unit
VCOM output voltage	VCOM	-	VCOM	-	TBD	-	V
Positive Source output voltage	V _{SH}	-	S ₀ ~S ₁₅₁	+14.5	+15	+15.5	V
Negative Source output voltage	V _{SL}	-	S ₀ ~S ₁₅₁	-15.5	-15	-14.5	V
Positive gate output voltage	V _{gh}	-	G ₀ ~G ₁₅₁	+21	+22	+23	V
Negative gate output voltage	V _{gl}	-	G ₀ ~G ₁₅₁	-21	-20	-19	V

6.4 Panel AC Characteristics

6.4.1 MCU Interface Selection

The pin assignment at different interface mode is summarized in Table 6-4-1. Different MCU mode can be set by hardware selection on BS1 pins. The display panel only supports 4-wire SPI or 3-wire SPI interface mode.

Pin Name	Data/Command Interface		Control Signal		
	SDA	SCL	CS#	D/C#	RES#
Bus interface	SDA	SCL	CS#	D/C#	RES#
BS1=L 4-wire SPI	SDA	SCL	CS#	D/C#	RES#
BS1=H 3-wire SPI	SDA	SCL	CS#	L	RES#

6.4.2 MCU Serial Interface (4-wire SPI)

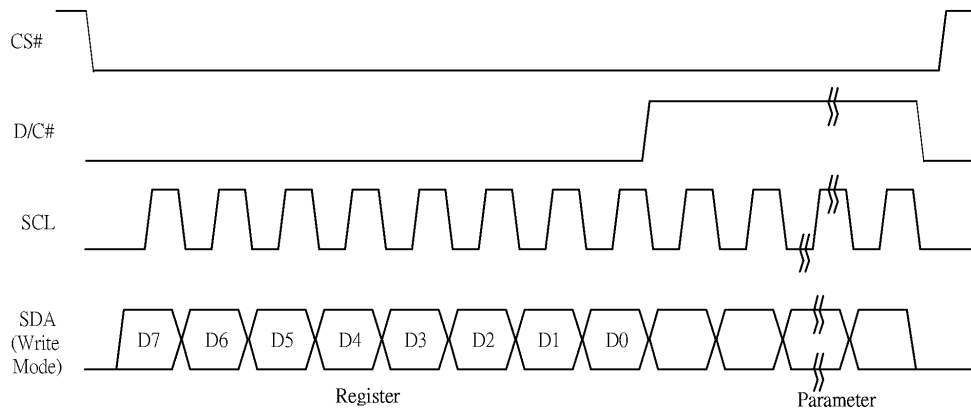
The serial interface consists of serial clock SCL, serial data SDA, D/C#, CS#. This interface supports Write mode and Read mode.

Function	CS#	D/C#	SCL
Write command	L	L	↑
Write data	L	H	↑

Note: ↑ stands for rising edge of signal

In the write mode SDA is shifted into an 8-bit shift register on every rising edge of SCL in the order of D7, D6, ... D0. The level of D/C# should be kept over the whole byte. The data byte in the shift register is written to the Graphic Display Data RAM /Data Byte register or command Byte register according to D/C# pin.

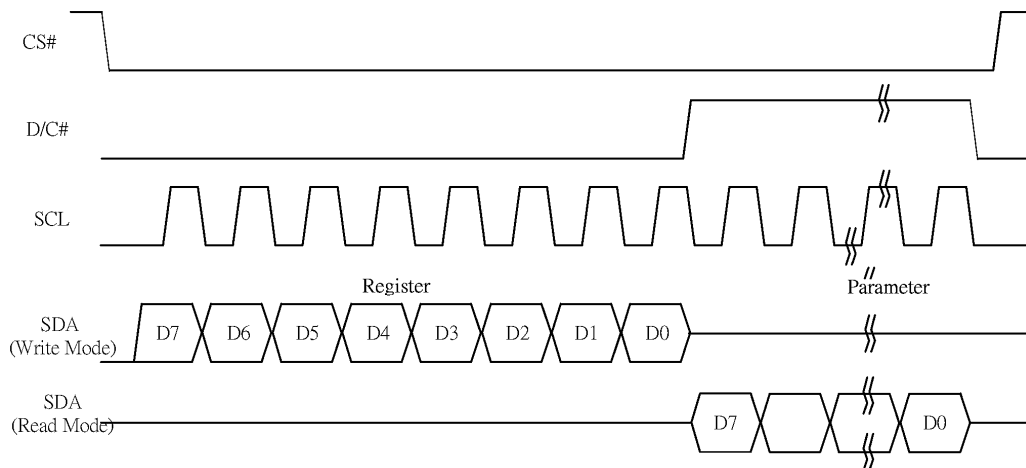
Figure 6-1: Write procedure in 4-wire SPI mode



In the Read mode:

1. After driving CS# to low, MCU need to define the register to be read.
2. SDA is shifted into an 8-bit shift register on every rising edge of SCL in the order of D7, D6, ... D0 with D/C# keep low.
3. After SCL change to low for the last bit of register, D/C# need to drive to high.
4. SDA is shifted out an 8-bit data on every falling edge of SCL in the order of D7, D6, ... D0.
5. Depending on register type, more than 1 byte can be read out. After all byte are read, CS# need to drive to high to stop the read operation.

Figure 6-2: Read procedure in 4-wire SPI mode



6.4.3 MCU Serial Interface (3-wire SPI)

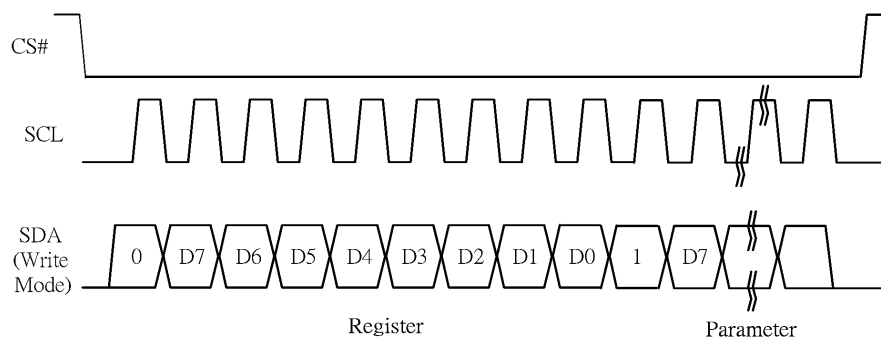
The 3-wire serial interface consists of serial clock SCL, serial data SDA and CS#. This interface also supports Write mode and Read mode.

The operation is similar to 4-wire serial interface while D/C# pin is not used. There are altogether 9-bits will be shifted into the shift register on every ninth clock in sequence: D/C# bit, D7 to D0 bit. The D/C# bit (first bit of the sequential data) will determine the following data byte in the shift register is written to the Display Data RAM (D/C# bit = 1) or the command register (D/C# bit = 0).

Function	CS#	D/C#	SCL
Write command	L	Tie	↑
Write data	L	Tie	↑

Note: ↑ stands for rising edge of signal

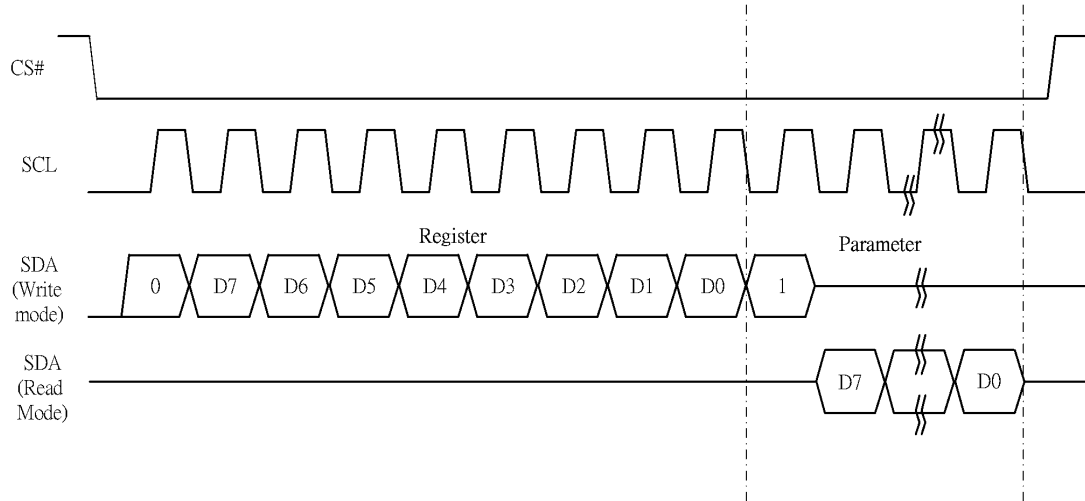
Figure 6-3: Write procedure in 3-wire SPI mode



In the Read mode:

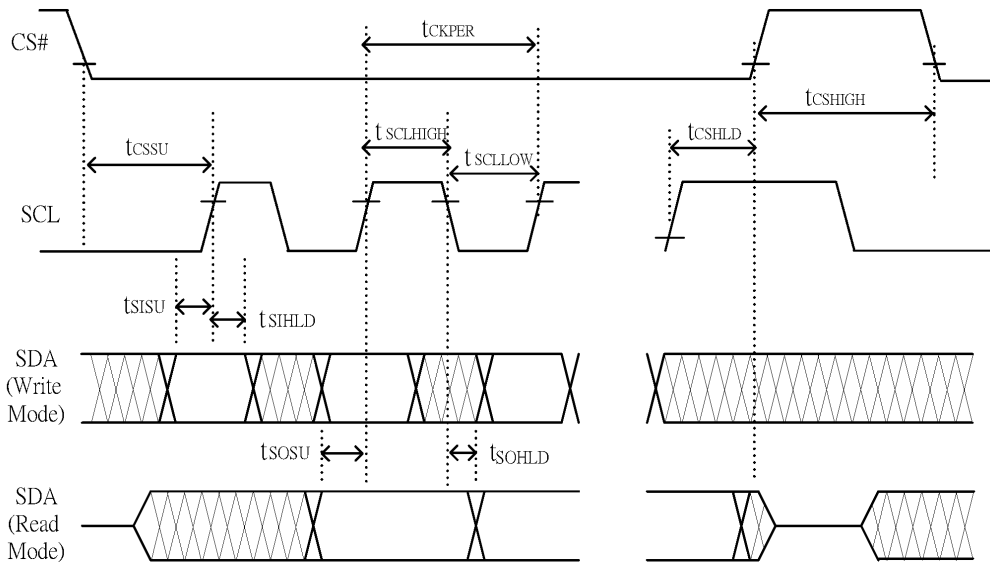
1. After driving CS# to low, MCU need to define the register to be read.
2. D/C=0 is shifted thru SDA with one rising edge of SCL
3. SDA is shifted into an 8-bit shift register on every rising edge of SCL in the order of D7, D6, ... D0.
4. D/C=1 is shifted thru SDA with one rising edge of SCL
5. SDA is shifted out an 8-bit data on every falling edge of SCL in the order of D7, D6, ... D0.
6. Depending on register type, more than 1 byte can be read out. After all byte are read, CS# need to drive to high to stop the read operation.

Figure 6-4: Read procedure in 3-wire SPI mode



6.4.4 Interface Timing

The following specifications apply for: VSS=0V, VCI=3.0V, T_{OPR} =23°C.



Changed Diagram

Serial Interface Timing Characteristics

(VCI - VSS = 2.2V to 3.7V, TOPR = 23°C, CL=20pF)

Write mode

Symbol	Parameter	Min	Typ.	Max	Unit
fSCL	SCL frequency (Write Mode)			20	MHz
tCSSU	Time CS# has to be low before the first rising edge of SCLK	60			ns
tCSHLD	Time CS# has to remain low after the last falling edge of SCLK	65			ns
tCSHIGH	Time CS# has to remain high between two transfers	100			ns
tSCLHIGH	Part of the clock period where SCL has to remain high	25			ns
tSCLLOW	Part of the clock period where SCL has to remain low	25			ns
tSISU	Time SI (SDA Write Mode) has to be stable before the next rising edge of SCL	10			ns
tSIHLD	Time SI (SDA Write Mode) has to remain stable after the rising edge of SCL	40			ns

Read mode

Symbol	Parameter	Min	Typ.	Max	Unit
fSCL	SCL frequency (Read Mode)			2.5	MHz
tCSSU	Time CS# has to be low before the first rising edge of SCLK	100			ns
tCSHLD	Time CS# has to remain low after the last falling edge of SCLK	50			ns
tCSHIGH	Time CS# has to remain high between two transfers	250			ns
tSCLHIGH	Part of the clock period where SCL has to remain high	180			ns
tSCLLOW	Part of the clock period where SCL has to remain low	180			ns
tSOSU	Time SO(SDA Read Mode) will be stable before the next rising edge of SCL		50		ns
tSOHLD	Time SO (SDA Read Mode) will remain stable after the failing edge of SCL		0		ns

7.Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	01	0	0	0	0	0	0	0	1	Driver	Gate setting Set A[8:0]=0097h Set B[8:0]=00h
0	1		A7	A6	A5	A4	A3	A2	A1	A0	Output	
0	1		0	0	0	0	0	0	0	A8	control	
0	1		0	0	0	0	0	B2	B1	B0		
0	0	03	0	0	0	0	0	0	1	1	Gate	Set Gate Driving voltage A[4:0]=17h[POR], VGH at 20V[POR] VGH setting from 10V to 20V
0	1		0	0	0	A4	A3	A2	A1	A0	Driving voltage control	
0	0	04	0	0	0	0	0	1	0	0	Source	Set Source Driving voltage A[7:0]= 41h[POR], VSH1 at 15V B[7:0]=A Ch[POR], VSH2 at 5.4V C[7:0]= 32h[POR], VSL at -15V
0	1		A7	A6	A5	A4	A3	A2	A1	A0	Driving	
0	1		B7	B6	B5	B4	B3	B2	B1	B0	voltage control	
0	1		C7	C6	C5	C4	C3	C2	C1	C0		
0	0	08	0	0	0	0	1	0	0	0	Initial Code Setting OTP Program	Program Initial Code Setting The command required CLKEN=1. Refer to Register 0x22 for detail. BUSY pad will output high during operation
0	0	09	0	0	0	0	1	0	0	1	Write	Write Register for Initial Code Setting Selection A[7:0] ~ D[7:0]: Reserved Details refer to Application Notes of Initial Code Setting
0	1		A7	A6	A5	A4	A3	A2	A1	A0	Register	
0	1		B7	B6	B5	B4	B3	B2	B1	B0	for Initial	
0	1		C7	C6	C5	C4	C3	C2	C1	C0	Code	
0	1		D7	D6	D5	D4	D3	D2	D1	D0	Setting	
0	0	0A	0	0	0	0	1	0	1	0	Read Register for Initial Code Setting	Read Register for Initial Code Setting
0	0	10	0	0	0	1	0	0	0	0	Deep	Deep Sleep mode Control: A[1:0] : Description 00 Normal Mode [POR] 01 Enter Deep Sleep Mode 1 11 Enter Deep Sleep Mode 2 After this command initiated, the chip will enter Deep Sleep Mode, BUSY pad will keep output high. Remark: To Exit Deep Sleep mode, User required to send HWRESET to the driver
0	1		0	0	0	0	0	0	0	A0	Sleep mode	
0	0	11	0	0	0	1	0	0	0	1	Data Entry mode setting	Define data entry sequence A[2:0] = 011 [POR] A [1:0] = ID[1:0] Address automatic increment / decrement setting The setting of incrementing or decrementing of the address counter can be made independently in each upper and

0	1		0	0	0	0	0	A ₂	A ₁	A ₀			
0	0	0C	0	0	0	0	1	1	0	0	Booster Soft start Control	Booster Enable with Phase 1, Phase 2 and Phase 3 for soft start current and duration setting. A[7:0] -> Soft start setting for Phase1 = 8Bh [POR] B[7:0] -> Soft start setting for Phase2 = 9Ch [POR] C[7:0] -> Soft start setting for Phase3 = 96h [POR] D[7:0] -> Duration setting = 0Fh [POR] Bit Description of each byte: A[6:0] / B[6:0] / C[6:0]: Bit[6:4] Driving Strength Selection 000 1(Weakest) 001 2 010 3 011 4 100 5 101 6 110 7 111 8(Strongest) Bit[3:0] Min Off Time Setting of GDR [Time unit] 0000 ~ 0011 NA 0100 2.6 0101 3.2 0110 3.9 0111 4.6 1000 5.4 1001 6.3 1010 7.3 1011 8.4 1100 9.8	
0	1		1	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀			
0	1		1	B ₆	B ₅	B ₄	B ₃	B ₂	B ₁	B ₀			
0	1		1	C ₆	C ₅	C ₄	C ₃	C ₂	C ₁	C ₀			
0	1		0	0	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀			

0	1		B7	0	0	0	0	0	0	0		
0	0	22	0	0	1	0	0	0	1	0	Display Update Control 2	Display Update Sequence Option: Enable the stage for Master Activation A[7:0]= FFh (POR) Operating sequence Parameter (in Hex) Enable clock signal 80 Disable clock signal 01 Enable clock signal Enable Analog C0 Disable Analog Disable clock signal 03 Enable clock signal Load LUT with DISPLAY Mode 1 Disable clock signal 91 Enable clock signal Load LUT with DISPLAY Mode 2 Disable clock signal 99 Enable clock signal Load temperature value Load LUT with DISPLAY Mode 1 Disable clock signal B1 Enable clock signal Load temperature value Load LUT with DISPLAY Mode 2 Disable clock signal B9 Enable clock signal Enable Analog Display with DISPLAY Mode 1 Disable Analog Disable OSC C7 Enable clock signal Enable Analog Display with DISPLAY Mode 2 Disable Analog Disable OSC
0	1		A7	A6	A5	A4	A3	A2	A1	A0		

0	0	24	0	0	1	0	0	1	0	0	Write RAM (Black White) / RAM 0x24	After this command, data entries will be written into the BW RAM until another command is written. Address pointers will advance accordingly For Write pixel: Content of Write RAM(BW) = 1 For Black pixel: Content of Write RAM(BW) = 0
0	0	26	0	0	1	0	0	1	1	0	Write RAM (RED) / RAM 0x26)	After this command, data entries will be written into the RED RAM until another command is written. Address pointers will advance accordingly. For Red pixel: Content of Write RAM(RED) = 1 For non-Red pixel [Black or White]: Content of Write RAM(RED) = 0
0	0	2C	0	0	1	0	1	1	0	0	Write VCOM register	Write VCOM register from MCU interface A[7:0] = 00h [POR]
0	1		A7	A6	A5	A4	A3	A2	A1	A0		
0	0	2D	0	0	1	0	1	1	0	1	OTP Register Read for Display Option	Read Register for Display Option: A[7:0]: VCOM OTP Selection (Command 0x37, Byte A) B[7:0]: VCOM Register (Command 0x2C) C[7:0]~G[7:0]: Display Mode (Command 0x37, Byte B to Byte F) [5 bytes] H[7:0]~K[7:0]: Waveform Version (Command 0x37, Byte G to Byte J) [4 bytes]
1	1		A7	A6	A5	A4	A3	A2	A1	A0		
1	1		B7	B6	B5	B4	B3	B2	B1	B0		
1	1		C7	C6	C5	C4	C3	C2	C1	C0		
1	1		D7	D6	D5	D4	D3	D2	D1	D0		
1	1		E7	E6	E5	E4	E3	E2	E1	E0		
1	1		F7	F6	F5	F4	F3	F2	F1	F0		
1	1		G7	G6	G5	G4	G3	G2	G1	G0		
1	1		H7	H6	H5	H4	H3	H2	H1	H0		
1	1		I7	I6	I5	I4	I3	I2	I1	I0		
1	1		J7	J6	J5	J4	J3	J2	J1	J0		
1	1		K7	K6	K5	K4	K3	K2	K1	K0		
0	0	2F	0	0	1	0	1	1	1	1	Status Bit Read	Read IC status Bit [POR 0x01] A[5]: HV Ready Detection flag [POR=0] 0: Ready 1: Not Ready A[4]: VCI Detection flag [POR=0] 0: Normal 1: VCI lower than the Detect level A[3]: [POR=0] A[2]: Busy flag [POR=0] 0: Normal 1: BUSY A[1:0]: Chip ID [POR=01] Remark: A[5] and A[4] status are not valid after RESET, they need to be initiated by command 0x14 and command 0x15 respectively

0	0	30	0	0	1	1	0	0	0	0	Program WS OTP	Program OTP of Waveform Setting The contents should be written into RAM before sending this command. The command required CLKEN=1. Refer to Register 0x22 for detail. BUSY pad will output high during operation
0	0	32	0	0	1	1	0	0	1	0	Write LUT register	Write LUT register from MCU interface [153 bytes], which contains the content of VS[nX-LUTm], TP[nX], RP[n], SR[nXY], FR[n] and XON[nXY] Refer to Session 6.7 WAVEFORM SETTING
0	1		A7	A6	A5	A4	A3	A2	A1	A0		
0	1		B7	B6	B5	B4	B3	B2	B1	B0		
0	1		:	:	:	:	:	:	:	:		
0	1		:	:	:	:	:	:	:	:		
0	1		:	:	:	:	:	:	:	:		
0	1		:	:	:	:	:	:	:	:		
0	0	39	0	0	1	1	1	0	0	1	OTP program mode	OTP program mode A[1:0] = 00: Normal Mode [POR] A[1:0] = 11: Internal generated OTP programming voltage Remark: User is required to EXACTLY follow the reference code sequences
0	0	3C	0	0	1	1	1	1	0	0		Select border waveform for VBD

0	1		A ₇	A ₆	A ₅	A ₄	0	0	A ₁	A ₀		A[7:0] = C0h [POR], set VBD as HIZ. A [7:6] :Select VBD option A[7:6] Select VBD as 00 GS Transition, Defined in A[2] and A[1:0] 01 Fix Level, Defined in A[5:4] 10 VCOM 11[POR] HiZ A [5:4] Fix Level Setting for VBD A[5:4] VBD level 00 VSS 01 VSH1 10 VSL 11 VSH2 A[2] GS Transition control A[2] GS Transition control 0 Follow LUT (Output VCOM @ RED) 1 Follow LUT A [1:0] GS Transition setting for VBD A[1:0] VBD Transition 00 LUT0 01 LUT1 10 LUT2 11 LUT3
0	0	44	0	1	0	0	0	1	0	0	Set RAM X - address Start / End position	Specify the start/end positions of the window address in the X direction by an address unit A[4:0]: XSA[4:0], X Start, POR = 00h B[4:0]: XEA[4:0], X End, POR = 0Ch
0	1		0	0	0	A ₄	A ₃	A ₂	A ₁	A ₀		
0	1		0	0	0	B ₄	B ₃	B ₂	B ₁	B ₀		
0	0	45	0	1	0	0	0	1	0	1	Set Ram Y- address Start / End position	Specify the start/end positions of the window address in the Y direction by an address unit A[8:0]: YSA[8:0], Y Start, POR = 00D3h B[8:0]: YEA[8:0], Y End, POR = 0000h
0	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		
0	1		0	0	0	0	0	0	0	A ₈		
0	1		B ₇	B ₆	B ₅	B ₄	B ₃	B ₂	B ₁	B ₀		
0	0	4E	0	1	0	0	1	1	1	0	Set RAM X address counter	Make initial settings for the RAM X address in the address counter (AC) A[4:0]: XAD[4:0], POR is 00h
0	1		0	0	0	A ₄	A ₃	A ₂	A ₁	A ₀		
0	0	4F	0	1	0	0	1	1	1	1	Set RAM Y address counter	Make initial settings for the RAM Y address in the address counter (AC) A[8:0]: YAD[8:0], POR is 00D3h
0	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		
0	1		0	0	0	0	0	0	0	A ₈		

8. Optical Specification

Measurements are made with that the illumination is under an angle of 45 degree, the detection is perpendicular unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ.	Max	Units	Notes
R	White Reflectivity	White	30	35	-	%	8-1
CR	Contrast Ratio	indoor	8:1		-		8-2
GN	2Grey Level	-	-	$DS+(WS-DS)*n(m-1)$			8-3
T update	Image update time	at 23 °C	-	14	-	sec	
Life		25±3°C 55±10%RH		5years			

Notes: 8-1. Luminance meter: Eye-One Pro Spectrophotometer.

8-2. CR=Surface Reflectance with all white pixel/Surface Reflectance with all black pixels.

8-3 WS: White state, DS: Dark state

9. Handling, Safety, and Environment Requirements

Warning

The display glass may break when it is dropped or bumped on a hard surface. Handle with care. Should the display break, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap.

Caution

The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components. Disassembling the display module.

Disassembling the display module can cause permanent damage and invalidates the warranty agreements.

Observe general precautions that are common to handling delicate electronic components. The glass can break and front surfaces can easily be damaged. Moreover the display is sensitive to static electricity and other rough environmental conditions.

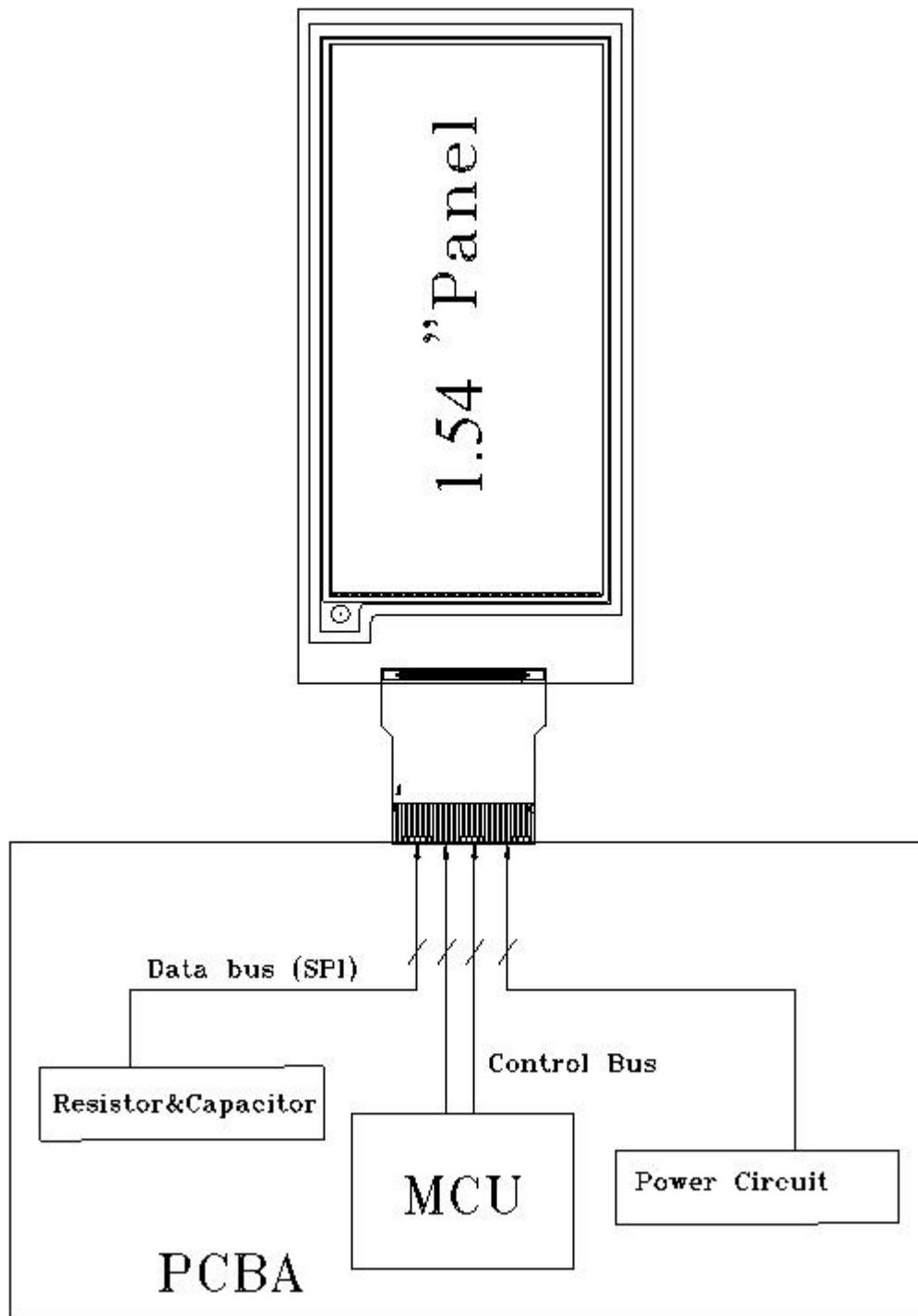
Data sheet status	
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

10. Reliability Test

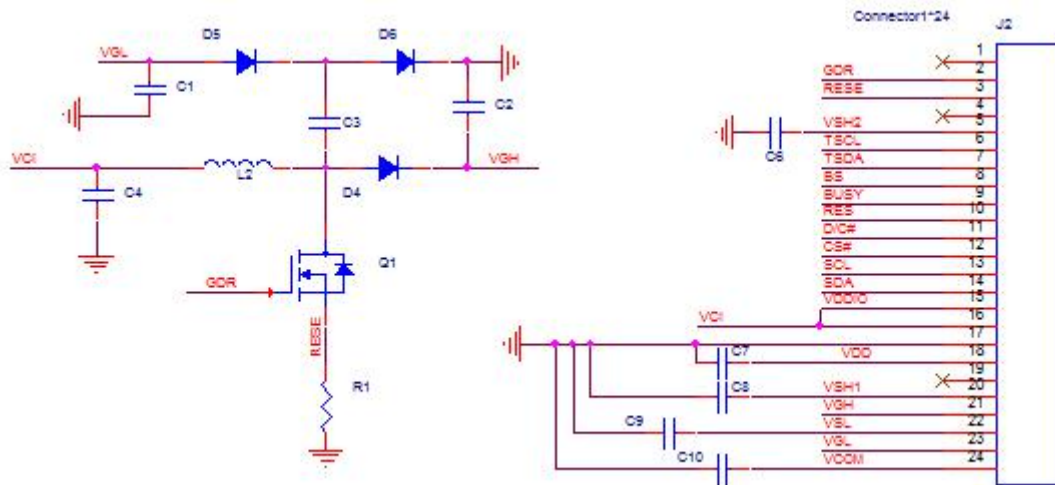
NO	Test items	Test condition
1	Low-Temperature Storage	T = -25°C, 240 h Test in white pattern
2	High-Temperature Storage	T=60°C, RH=40%, 240h Test in white pattern
3	High-Temperature Operation	T=40°C, RH=35%, 240h
4	Low-Temperature Operation	0°C, 240h
5	High-Temperature, High-Humidity Operation	T=40°C, RH=80%, 240h
6	High Temperature, High Humidity Storage	T=50°C, RH=80%, 240h Test in white pattern
7	Temperature Cycle	1 cycle:[-25°C 30min]→[+60 °C 30 min] : 50 cycles Test in white pattern
8	UV exposure Resistance	765W/m ² for 168hrs,40 °C Test in white pattern
9	ESD Gun	Air+/-15KV;Contact+/-8KV (Test finished product shell, not display only) Air+/-8KV;Contact+/-6KV (Naked EPD display, no including IC and FPC area) Air+/-4KV;Contact+/-2KV (Naked EPD display, including IC and FPC area)

Note: Put in normal temperature for 1hour after test finished, display performance is ok.

11. Block Diagram



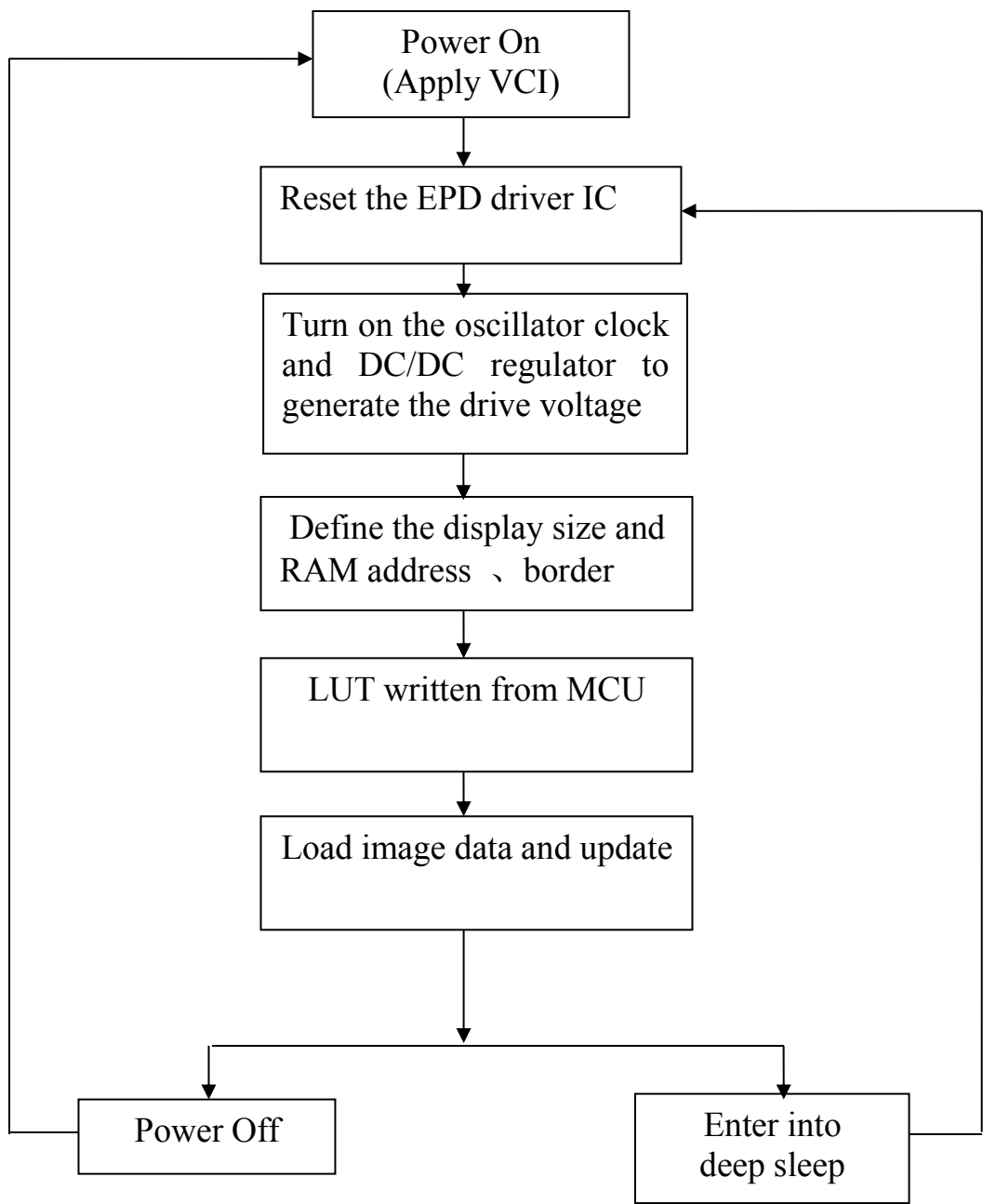
12. Typical Application Circuit with SPI Interface



Part Name	Value	Reference Part	Requirements for spare part
C4 C7	1uF	0603;X5R/X7R;Voltage Rating:6v or 25v	
C1 C2 C3 C6 C8 C9	1uF	0603/0805; X5R/X7R;Voltage Rating:25v	
C10	0.47uF/1 uF	0603/0805; X7R;Voltage Rating:25v NOTE: Effective capacitance >0.25uF @18v DC bias	
R1	2.2Ohm	0805; 1%	
D4 D5 D6	Diode	MBR0530	1)Reverse DC Voltage=30V(max) 2)Io=500mA 3)Forward voltage =430mV(max)
Q1	NMOS	Si1304BDL/NX3008N13K	1)Drain-Source breakdown voltage =30v(min) 2)Vgs(th)=0.9v(Typ), 1.3v(Max) 3)rds on≤2.1Ω@ Vgs=2.5v
L2	47UH	CDRH2D18/LDNP-470NC	1) Io=500(max)

13 Typical Operating Sequence

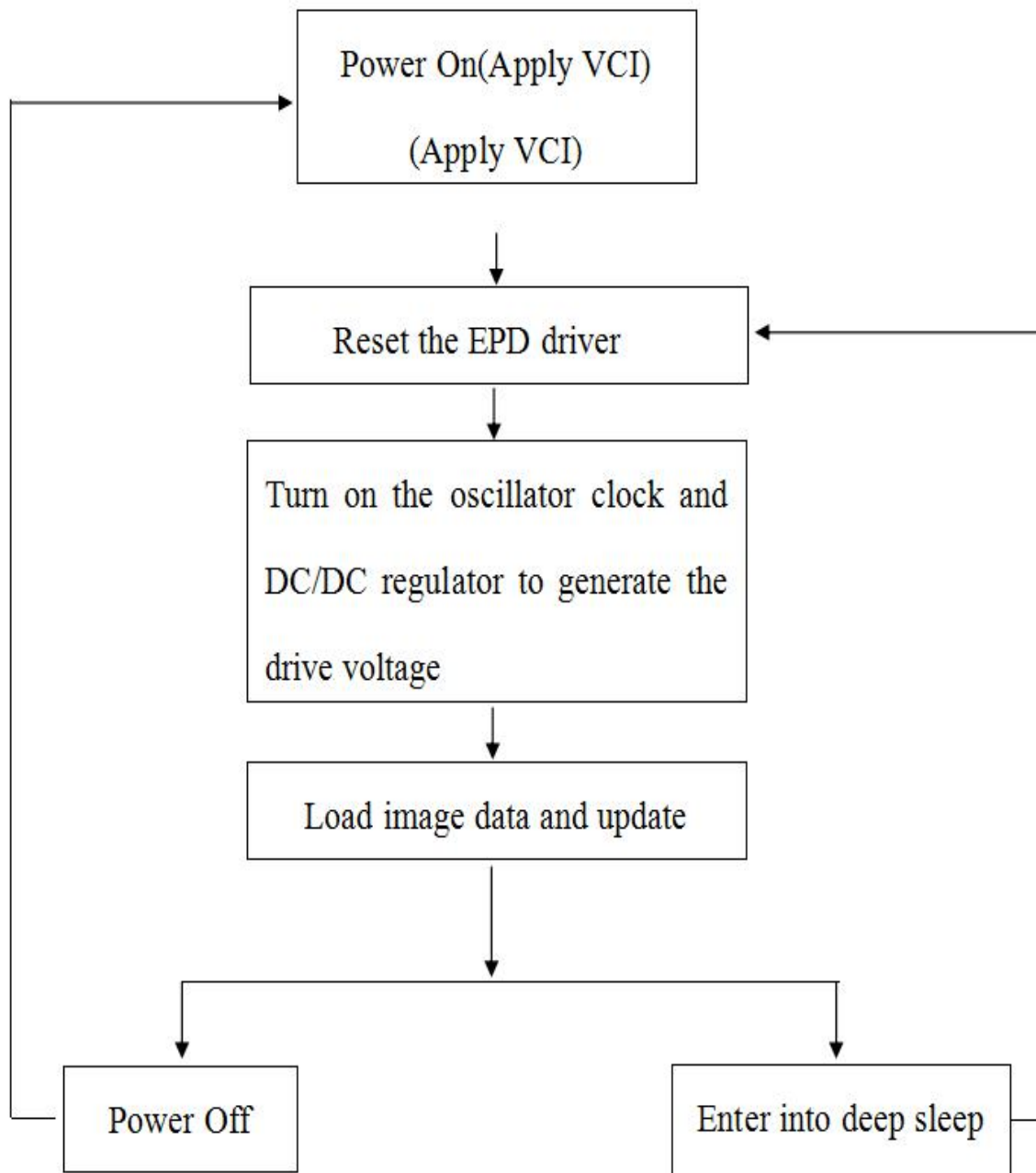
13.1 Normal Operation Flow



13.2 Normal Operation Reference Program Code

ACTION	VALUE/DATA	COMMENT
POWER ON		
delay	10ms	
PIN CONFIG		
RESE#	low	Hardware reset
delay	200us	
RESE#	high	
delay	200us	
Read busy pin		Wait for busy low
Command 0x12		Software reset
Read busy pin		Wait for busy low
Command 0x01	Data 0x97 0x00 0x00	Set display size and driver output control
Command 0x11	Data 0x01	Ram data entry mode
Command 0x44	Data 0x01 0x13	Set Ram X address
Command 0x45	Data 0x97 0x00 0x00 0x00	Set Ram Y address
Command 0x3C	Data 0x05	Set border
SET VOLTAGE AND LOAD LUT		
Command 0x2C	Data 0x36	Set VCOM value
Command 0x03	Data 0x17	Gate voltage setting
Command 0x04	Data 0x41 0x00 0x32	Source voltage setting
Command 0x32	Write 153bytes LUT	Load LUT
LOAD IMAGE AND UPDATE		
Command 0x4E	Data 0x00	Set Ram X address counter
Command 0x4F	Data 0x97 0x00	Set Ram Y address counter
Command 0x24	2888bytes	Load image (152/8*152)(BW)
Command 0x26	2888bytes	Load image (152/8*152)(RED)
Command 0x22	Data 0XC7	Image update
Command 0x20		
Read busy pin		Wait for busy low
Command 0x10	Data 0X01	Enter deep sleep mode
POWER OFF		

13.3 OTP Operation Flow



13.4OTP Operation Reference Program Code

ACTION	VALUE/DATA	COMMENT
POWER ON		
delay	10ms	
PIN CONFIG		
RESE#	low	Hardware reset
delay	200us	
RESE#	high	
delay	200us	
Read busy pin		Wait for busy low
Command 0x12		Software reset
Read busy pin		Wait for busy low
SET VOLTAGE AND LOAD LUT		
LOAD IMAGE AND UPDATE		
Command 0x24	2888bytes	Load image (152/8*152)(BW)
Command 0x26	2888bytes	Load image (152/8*152)(RED)
Command 0x20		
Read busy pin		Wait for busy low
Command 0x10	Data 0X01	Enter deep sleep mode
POWER OFF		

14. Part Number Definition

DEP G 0154 R W S800 F6

1 2 3 4 5 6 7

- 1: DEP:Manufacturer
- 2: G:Dot matrix type
- 3: The E-paper size:1.54inch:0154
- 4: The color of E-paper:
B : Black/White R: Black/White/Red Y: Black/White/Yellow
- 5: OT range: N: Normal L/S: Low temperature H/W: High temperature
- 6: Driver type: internal temperature sensor
- 7: FPC type

15. Inspection condition

15.1 Environment

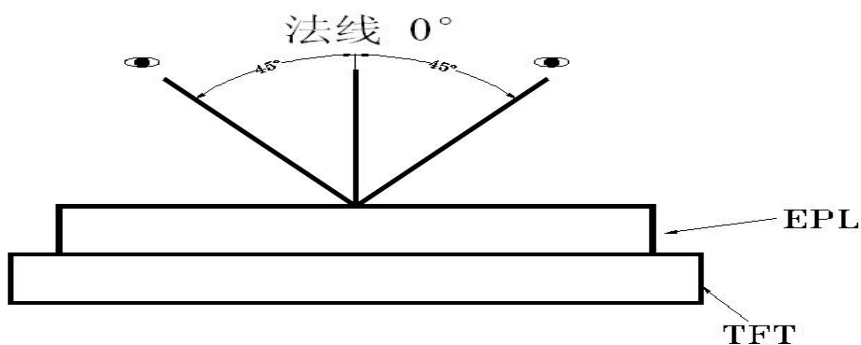
Temperature: $25\pm 3^{\circ}\text{C}$

Humidity: $55\pm 10\%\text{RH}$

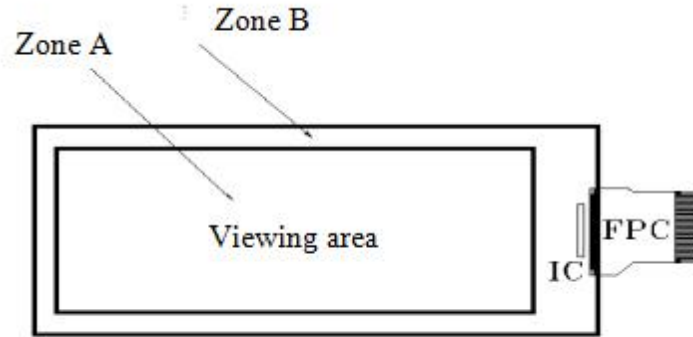
15.2 Illuminance

Brightness:1200~1500LUX;distance:20-30CM;Angle:Relate 45° surround.

15.3 Inspect method

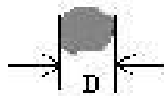
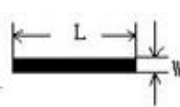


15.4 Display area



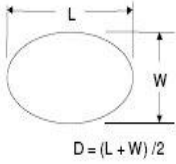
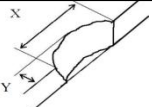
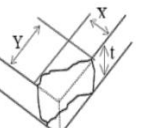
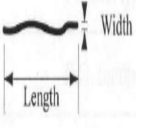

15.5 Inspection standard

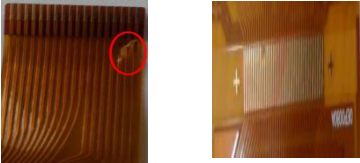
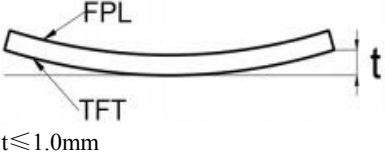
15.5.1 Electric inspection standard

NO.	Item	Standard	Defect level	Method	Scope
1	Display	Display complete Display uniform	MA		
2	Black/White spots	 $D \leq 0.25\text{mm}$, Allowed $0.25\text{mm} < D \leq 0.4\text{mm}$, $N \leq 4$, and Distance $\geq 5\text{mm}$ $0.4\text{mm} < D$ Not Allow	MI	Visual inspection	Zone A
3	Black/White spots (No switch)	 $L \leq 0.4\text{mm}$, $W \leq 0.1\text{mm}$ negligible $0.4\text{mm} < L \leq 1.0\text{mm}$ $0.1\text{mm} < W \leq 0.4\text{mm}$ $N \leq 4$ allowable $L > 1.0\text{mm}$, $W > 0.4\text{mm}$, Not Allow		Visual/ Inspection card	
4	Ghost image	Allowed in switching process	MI	Visual inspection	
5	Flash spots/ Larger FPL size	Flash spots in switching, Allowed FPL size larger than viewing area, Allowed	MI	Visual/ Inspection card	Zone A Zone B

6	Display wrong/Missing	All appointed displays are showed correct	MA	Visual inspection	Zone A
7	Short circuit/ Circuit break/ Display abnormal	Not Allow			

15.5.2 Appearance inspection standard

NO.	Item	Standard	Defect level	Method	Scope
1	B/W spots /Bubble/ Foreign bodies/ Dents	 $D = (L + W) / 2$ <p>$D \leq 0.25\text{mm}$, negligible $0.25\text{mm} < D \leq 0.4\text{mm}$, $N \leq 4$ Allowed $D > 0.4\text{mm}$, Not Allow</p>	MI	Visual inspection	Zone A
2	Glass crack	Not Allow	MA	Visual / Microscope	Zone A Zone B
3	Dirty	Allowed if can be removed	MI		Zone A Zone B
4	Chips/Scratch/ Edge crown	 <p>$X \leq 3\text{mm}$, $Y \leq 0.5\text{mm}$ And without affecting the electrode is permissible</p>  <p>$2\text{mm} \leq X$ or $2\text{mm} \leq Y$ Not Allow</p>  <p>$W \leq 0.1\text{mm}$, $L \leq 5\text{mm}$, No harm to the electrodes and $N \leq 2$ allow</p>	MI	Visual / Microscope	Zone A Zone B
5	TFT Cracks	 <p>Not Allow</p>	MA	Visual / Microscope	Zone A Zone B

6	Dirty/ foreign body	Allowed if can be removed/ allow	MI	Visual / Microscope	Zone A / Zone B
7	FPC broken/ Goldfingers oxidation/ scratch	 Not Allow	MA	Visual / Microscope	Zone B
8	TFT edge bulge /TFT chromatic aberration	TFT edge bulge: $X \leq 3\text{mm}$, $Y \leq 0.3\text{mm}$ Allowed TFT chromatic aberration :Allowed	MI	Visual / Microscope	Zone A Zone B
9	PCB damaged/ Poor welding/ Curl	PCB (Circuit area) damaged Not Allow PCB Poor welding Not Allow PCB Curl $\leq 1\%$			
10	Edge glue height/ Edge glue bubble	Edge Adhesives $H \leq PS$ surface (Including protect film) Edge adhesives seep in $\leq 1/2$ Margin width Length excluding Edge adhesives bubble: bubble Width $\leq 1/2$ Margin width; Length $\leq 5.0\text{mm}$. $n \leq 5$	MI	Visual / Ruler	Zone B
11	Protect film	Surface scratch but not effect protect function, Allowed		Visual Inspection	
12	Silicon glue	Thickness $\leq PS$ surface(With protect film): Full cover the IC; Shape: The width on the FPC $\leq 0.5\text{mm}$ (Front) The width on the FPC $\leq 1.0\text{mm}$ (Back) smooth surface, No obvious raised.	MI	Visual Inspection	
13	Warp degree (TFT substrate)	 $t \leq 1.0\text{mm}$	MI	Ruler	
14	Color difference in COM area (Silver point area)	Allowed		Visual Inspection	

16.Packaging

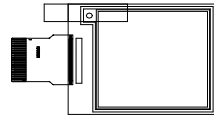
EPD PACKING INSTRUCTION				DATE	2017.03.28	
				DESIGN		
				CHECKED		
				APPROVED		

P/N	Customer Code	Ref. P/N	Type	PKG Method	Printing	Surface Marks	Pull Tape	Bar. Code
DEPG0154			GLASS	Blister	BACK	None	YES	None

Marks instruction:

print on the back of the product
Contents: model+Lot#

Pull tape:

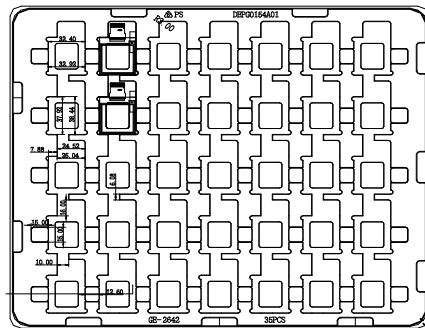


Packing Materials List					35PCS/LAYER, 20INNER BOX/CTN, TOTAL 700PCS/CTN.	
List	Model	Materials	Q'ty	Unit	Barcode Instruction:	
Carton	7#	corrugate	1	Piece		
BOX	7#(INNER)	corrugate	2	Piece		
Blister box	DEPG0154A01	PET	22	Piece		
Thin foam	298.4*273.92*T1.8-2.0	EPE	20	Piece		
Vaccum bag	450.0*590.0*0.075		2	Piece		
Foam board	DKE2251-10	EPE	5	Piece		
pull tape	16*5*T0.05		700	Piece		

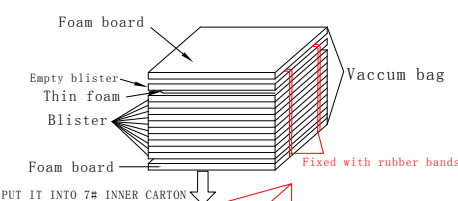
Detail:

Blister box:

NOTE:
TOTAL 10 LAYERS PER INNER BOX WITH ONE MORE EMPTY BLISTER ON THE TOP OF THE PRODUCTS.



Quantity: 5*7=35PCS



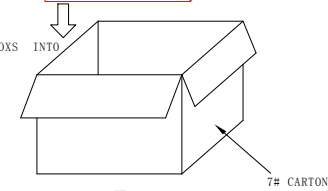
PUT IT INTO 7# INNER CARTON

INNER BOX LABEL

型号 (MODEL)	
数量 (QUANTITY)	
批号 (LOT)	

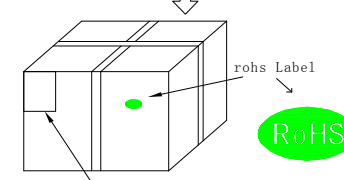
7# INNER BOX

PUT TWO 7# INNER BOXES INTO 7# CARTON



7# CARTON

Packing belt



Shipping marks according to customer's requirements

Epaper Identification	
QC:	PASS
Model No.	_____
Quantity	_____ pcs
Date:	_____
Carton No.	_____ of _____