N32G031 x6/x8 Datasheet

N32G031 Series Device, Arm® Cortex®-M0, Maximum operating frequency at 48MHz, Up to 64KB on-chip Flash Memory, 8KB SRAM, 1x12bit 1Msps ADC, 1xOPAMP, 1xCOMP, U(S)ART, I2C, SPI

Key features

- **Core**
  - A 32-bit general-purpose microcontroller based on the Arm® Cortex®-M0 core, Single-cycle hardware multiply instruction
  - 48MHz max
- **Encrypted memory**
  - Up to 64KByte on-chip Flash, supports encrypted storage, supports hardware ECC verification, Endurance more than 100,000 cycles, 10 years of data retention
  - 8KByte on-chip SRAM, supporting hardware parity
- **Low-power management**
  - Stop mode: RTC Run, maximum 16KByte Retention SRAM retention, CPU register retention, all IO retention
  - Power Down mode: support 3 IO wakeup
- **Clock**
  - HSE: 4MHz~20MHz external high-speed crystal
  - LSE: 32.768KHz external low-speed crystal
  - HSI: Internal high-speed RC OSC 8MHz
  - LSI: Internal low-speed RC OSC 30KHz
  - Built-in high-speed PLL
  - Mixed clock output (MCO), which can be configured as configurable system clock, HSE, HSI or PLL post-divided output
- **Reset**
  - Support power-on/power-down/external pin reset
  - Support programmable low voltage detection and reset
  - Support watchdog reset
- **Communication interface**
  - 3xU(S)ART, with a maximum rate of 3 Mbps, of which 2 USART interfaces (support 1xISO7816, 1xIrDA, LIN), 1 of which support low power consumption (LPUART, the highest communication rate in this mode is 9600bps) ,Stop mode can be awakened
  - 2xSPI, the rate is up to 18 MHz, one of which supports multiplexing with I2S
  - 2xI2C, the rate is up to 1 MHz, master-slave mode is configurable, and dual-address response is supported in slave mode
- **Analog interface**
  - 1x12bithigh-speed ADC, 1Msps, up to 12 external single-ended input channels
  - 1xOPAMP, built-in programmable gain amplifier up to 32 times
  - 1xCOMP, built-in 64-level adjustable comparison benchmark
- **Up to 40 GPIOs that support multiplexing functions.**

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- **1xDMA, 5-channel, source address and destination address of channel can be configured arbitrarily**
- **1xRTC, support leap year perpetual calendar, alarm event, periodic wake-up, support internal and external clock calibration**
- **1xBeeper, support complementary output, maximum drive capacity of 16mA**
- **Timer counter**
  - 2x16bit Advanced Timer, support input capture, complementary output, quadrature encoding input, 4 independent channels, of which 3 channels support 6 complementary PWM outputs
  - 1x16bit General Timer, 4 independent channels, supports input capture/output comparison/PWM output
  - 1x16bit Basic Timer
  - 1x16bit Low-Power Timer
  - 1x24bit SysTick
  - 1x7bit Window Watchdog (WWDG)
  - 1x12bit Independent watchdog (IWDG)
- **Programming method**
  - SWD online debugging interface
  - UART Bootloader
- **Hardware Divider(HDIV)and Square Root(SQRT)**
- **Security features**
  - Flash storage encryption
  - CRC16/32 calculation
  - Flash support write protection(WRP), multiple read protection(RDP) levels (L0/L1/L2)
  - Support clock failure monitoring, anti-dismantling monitoring
- **96-bit UID and 128-bit UCID**
- **Working conditions**
  - Operating Voltage Range: 1.8V~5.5V
  - Operating Temperature Range: -40℃~105℃
  - ESD: ±4KV (HBM model), ±1KV (CDM model)
- **Package**
  - UFQFPN20(3mm x 3mm)
  - TSSOP20(6.5mm x 4.4mm)
  - QFN32(4mm x 4mm)
  - QFN32(5mm x 5mm)
  - LQFP32(7mm x 7mm)
  - LQFP48(7mm x 7mm)
  - TQFP48(7mm x 7mm)
- **Order model**

Series	Part Number
N32G031x6 N32G031x8	N32G031F6U7, N32G031F6S7, N32G031K6L7, N32G031K6Q7, N32G031K6Q7-1,

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	N32G031F8U7, N32G031F8S7, N32G031K8L7, N32G031K8Q7, N32G031K8Q7-1, N32G031C8L7, N32G031C8T7,

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Table of contents

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List of table

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List of figures

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1 Product Brief

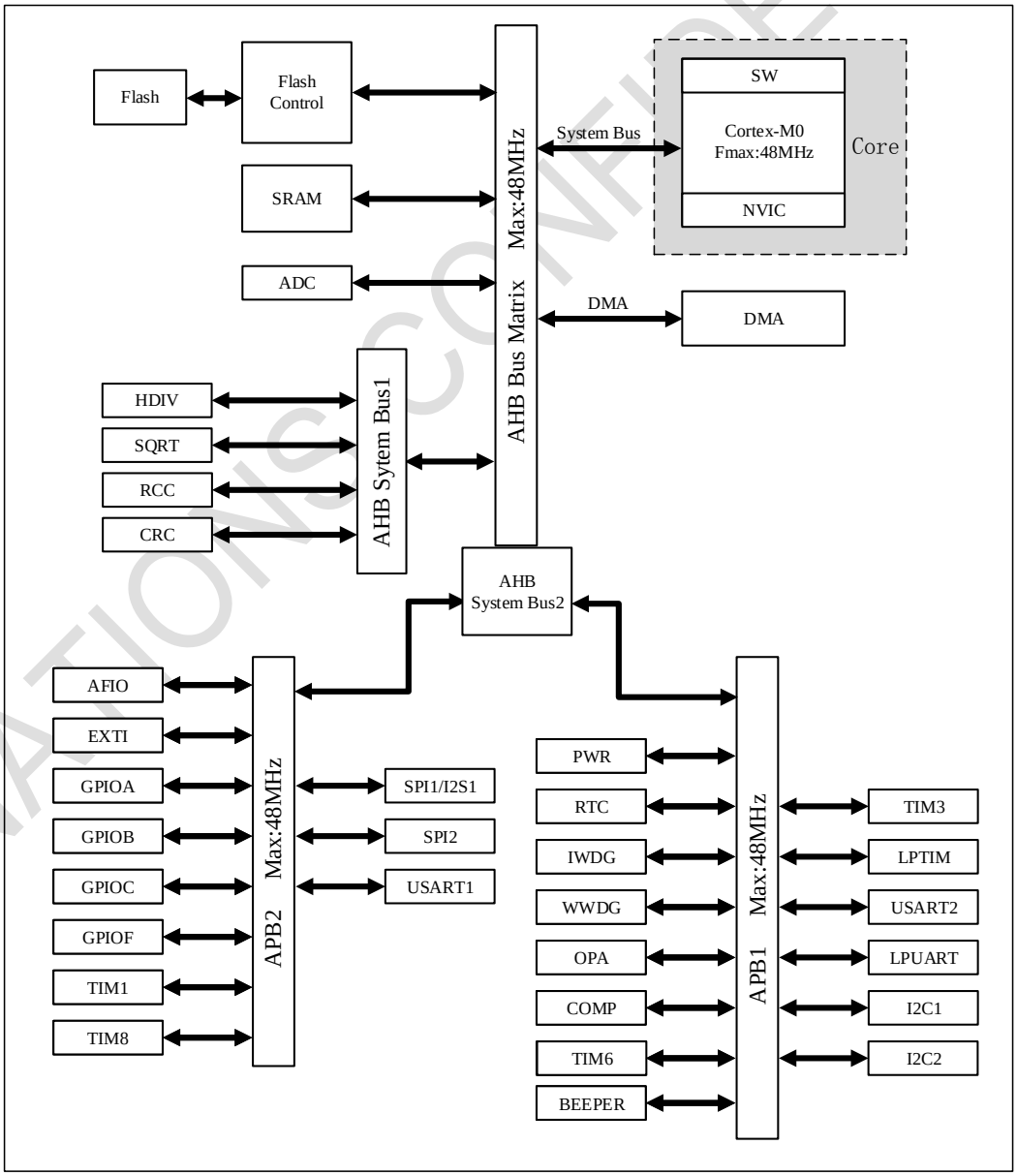
N32G031 microcontroller products use a 32-bit ARM Cortex®-M0 core with a maximum operating frequency of 48MHz, integrated up to 64KB of encrypted storage Flash, and a maximum of 8KB of SRAM; built-in a high-speed AHB bus, two low-speed peripheral buses APB and bus matrix, Supports up to 40 general-purpose I/Os, provides a wealth of high-performance analog interfaces, including 1x12-bit 1Msps ADC, supports up to 12 external input channels, 1 independent operational amplifier, 1 high-speed comparator, and provides multiple Digital communication interface, including 3xU(S)ART, 2xI2C, 2xSPI, 1xI2S.

N32G031 can work stably in the temperature range of -40 ℃ to +105 ℃, with a power supply voltage of 1.8V to 5.5V, and provide a variety of power consumption modes for users to choose from, meeting the requirements of low-power applications. This series of products provide different packages ranging from 20-pin to 48-pin. According to different package forms, the peripheral configurations in the device are not the same.

N32G031 series microcontrollers are suitable for multiple application scenarios such as mobile phone mobile devices, home appliance applications, motor control, balance cars, power management systems, etc.

Figure 1-1 shows the bus block diagram of this series of products.

Figure 1-1 N32G031 Block Diagram



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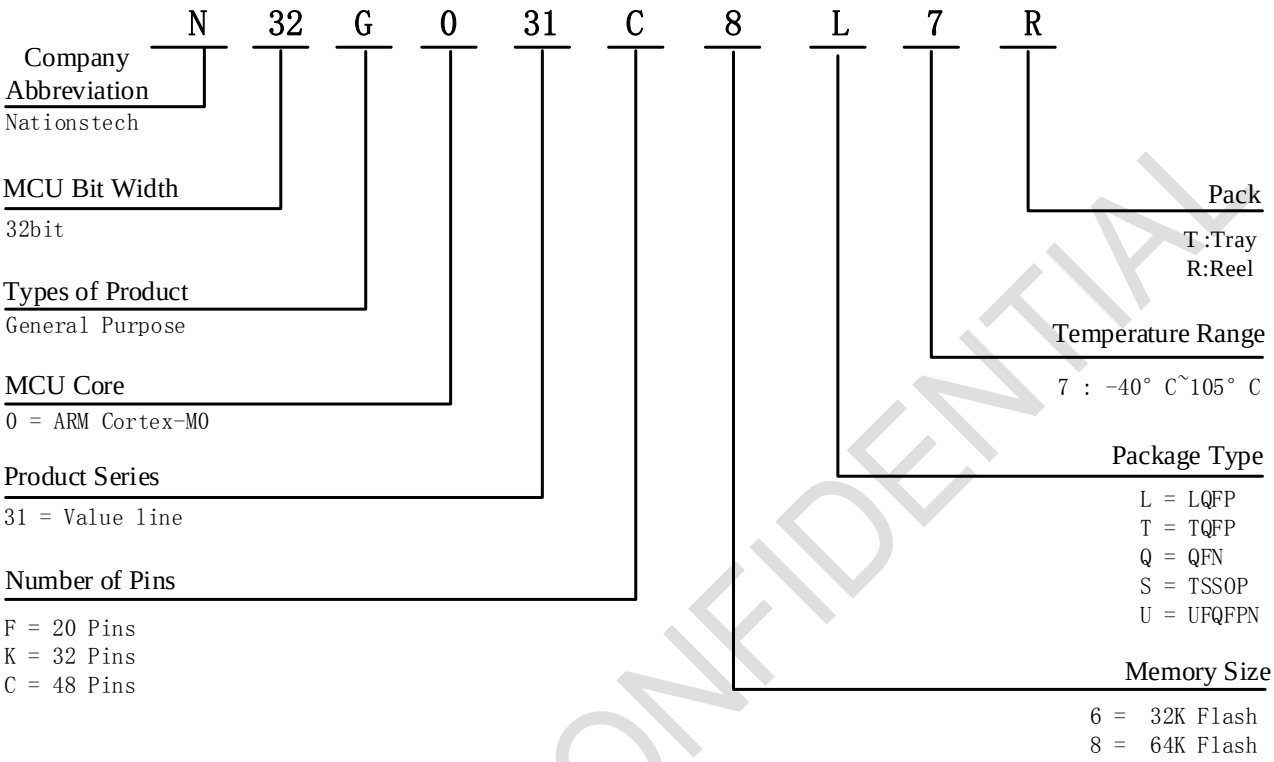
1.1 Naming rule

Figure 1-2 N32G031 Series Order code information



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1.2 Device information

Table 1-1 N32G031 Series devices features and peripheral list(1)

Part Number		N32G031 F8U7	N32G031 F8S7	N32G031 K8Q7	N32G031 K8Q7-1	N32G031 K8L7	N32G031 C8L7	N32G031 C8T7
Flash capacity (KB)		64	64	64	64	64	64	64
SRAM capacity (KB)		8	8	8	8	8	8	8
CPU frequency		ARM Cortex-M0 @48MHz						
working environment		1.8~5.5V/-40~105 ℃						
Timer	General	1						
	Advanced	2						
	Basic	1						
	LPTIM	1						
	RTC	1						
communication interface	SPI	2						
	I2S	1						
	I2C	2						
	USART	2						
	LPUART	1						
GPIO		16		28		26	40	
DMA Number of Channels		5						
12bit ADC Number of channels		1x12bit 7Channel	1x12bit 9Channel	1x12bit 10Channel			1x12bit 12Channel	
OPA/COMP		1/1						
Beeper		1						
Algorithm support		CRC16/CRC32						
security protection		Read and write protection (RDP/WRP), storage encryption						
Package		UFQFPN20	TSSOP20	QFN32 (5mx5m)	QFN32 (4mx4m)	LQFP32	LQFP48	TQFP48

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Table 1-2 N32G031 Series devices features and peripheral list(2)

Part Number		N32G031 F6U7	N32G031 F6S7	N32G031 K6Q7	N32G031 K6Q7-1	N32G031 K6L7
Flash capacity (KB)		32	32	32	32	32
SRAM capacity (KB)		8	8	8	8	8
CPU frequency		ARM Cortex-M0 @48MHz				
working environment		1.8~5.5V/-40~105℃				
Timer	General	1				
	Advanced	2				
	Basic	1				
	LPTIM	1				
	RTC	1				
communication interface	SPI	2				
	I2S	1				
	I2C	2				
	USART	2				
	LPUART	1				
GPIO		16		28		26
DMA Number of Channels		5				
12bit ADC Number of channels		1x12bit 7Channel	1x12bit 9Channel	1x12bit 10Channel		
OPA/COMP		1/1				
Beeper		1				
Algorithm support		CRC16/CRC32				
security protection		Read and write protection (RDP/WRP), storage encryption				
Package		UFQFPN20	TSSOP20	QFN32 (5mx5m)	QFN32 (4mx4m)	LQFP32

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2 Functional description

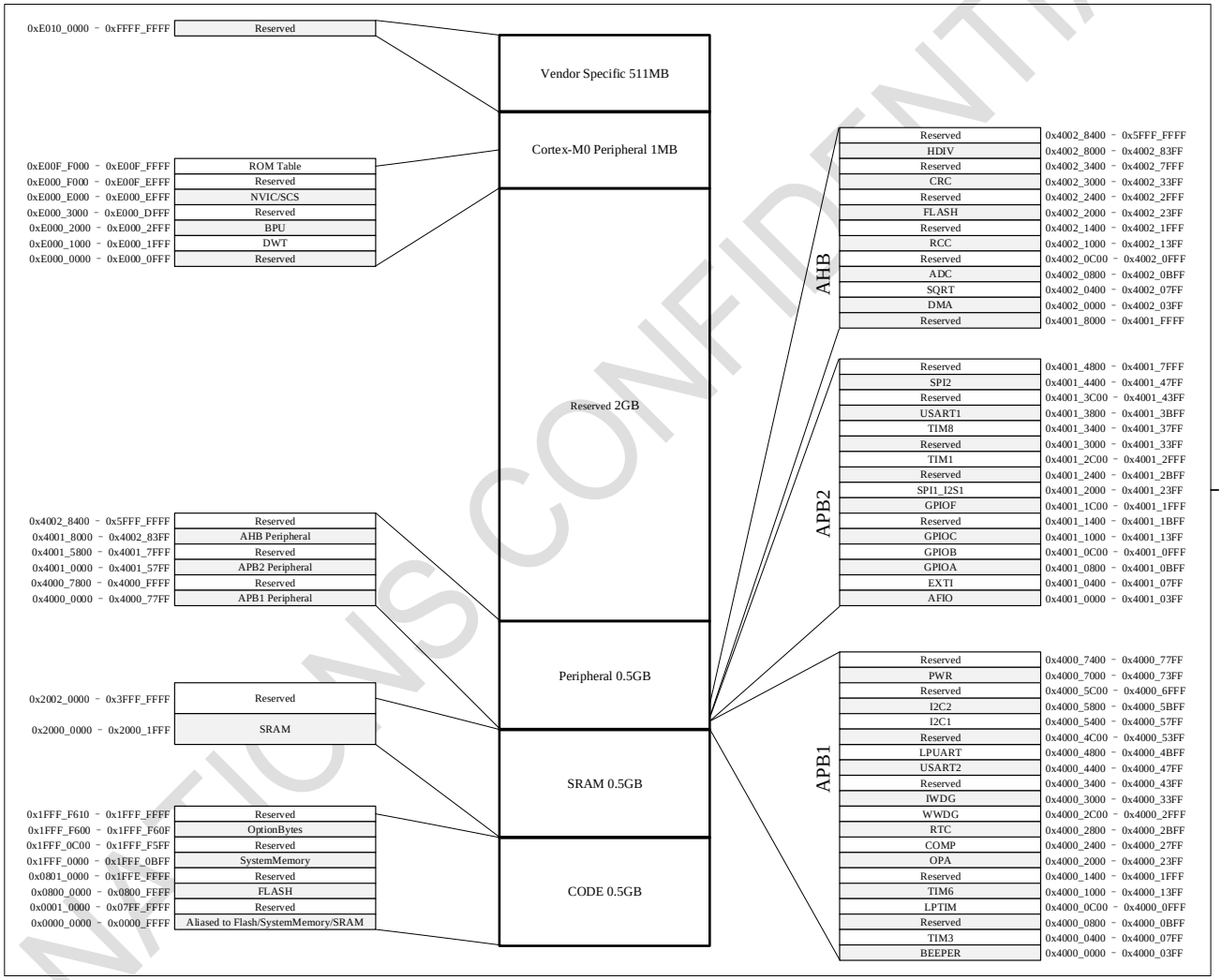
2.1 Core

N32G031 series integrates the latest generation of embedded ARM Cortex®-M0 processor

2.2 Memory

N32G031 series devices include embedded encrypted flash memory (Flash) and embedded SRAM, Figure 2-1 below shows the memory address map.

Figure 2-1 Memory address map



2.2.1 Embedded flash memory

The chip integrates 32K to 64K bytes of embedded flash memory (FLASH) for storing programs and data. The page size is 512byte and supports page erase, word write, word read, half-word read, and byte read operations.

Support storage encryption protection, write automatic encryption, read automatic decryption (including program execution operations).

2.2.2 Embedded SRAM

Up to 8K bytes of built-in SRAM is integrated on-chip, and data can be maintained in the STOP mode.

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2.2.3 Nested vectored interrupt controller (NVIC)

The Nested Vectored Interrupt Controller (NVIC) is closely connected to the interface of the processor core, which can realize low-latency interrupt processing and efficiently handle late-arriving interrupts. The nested vectored interrupt controller manages interrupts including kernel exceptions.

- 32 maskable interrupt channels (not including 16 Cortex®-M0 interrupt lines)
- 4 programmable priority levels (using 2-bit interrupt priority levels)
- Low-latency exception and interrupt handling
- Power management control
- Realization of system control register

The module provides flexible interrupt management functions with minimal interrupt delay

2.3 Extended interrupt/event controller (EXTI)

The extended interrupt/event controller includes 24 edge detection circuits that generate interrupts/event triggers. Each input line can be independently configured as an event or interrupt, as well as three trigger types of rising edge, falling edge or both edges, and can also be independently shielded. The suspend register holds the interrupt request of the status line, and the corresponding bit of the suspend register can be cleared by writing '1'.

2.4 Clock

The clock of the device includes internal high-speed RC oscillator HSI (8MHz), internal low-speed clock LSI (30KHz), external high-speed clock HSE (4MHz~20MHz), external low-speed clock (32.768KHz), PLL.

The system clock (SYSCLK) can choose the following clock sources:

- HSI
- HSE
- PLL
- LSI
- LSE

Secondary clock source:

- 30KHz low-speed internal RC, which can be used as the clock source of IWDG, RTC, LPTIMER and LPUART. Used to automatically wake up the system from STOP mode.
- 32.768KHz low-speed external crystal can also be used as the clock source of RTC, LPTIMER and LPUART.
- When not in use, any clock source can be independently shut down to reduce system power consumption.

The HSI clock is selected as the default system clock during reset, and then the user can select the HSE clock with failure monitoring function; when the HSE clock failure is detected, the system clock will automatically switch to HSI. If the interrupt is enabled, the corresponding interrupt can be generated. When needed, it is possible to take safe interrupt management of the PLL clock (for example, when the HSE used indirectly fails).

Users can configure the frequency of AHB and APB (APB1 and APB2) domains through multiple prescalers. The maximum allowable frequency of AHB domain, APB1 domain and APB2 domain is 48MHz.Figure 2-2 is a block diagram of the clock tree.

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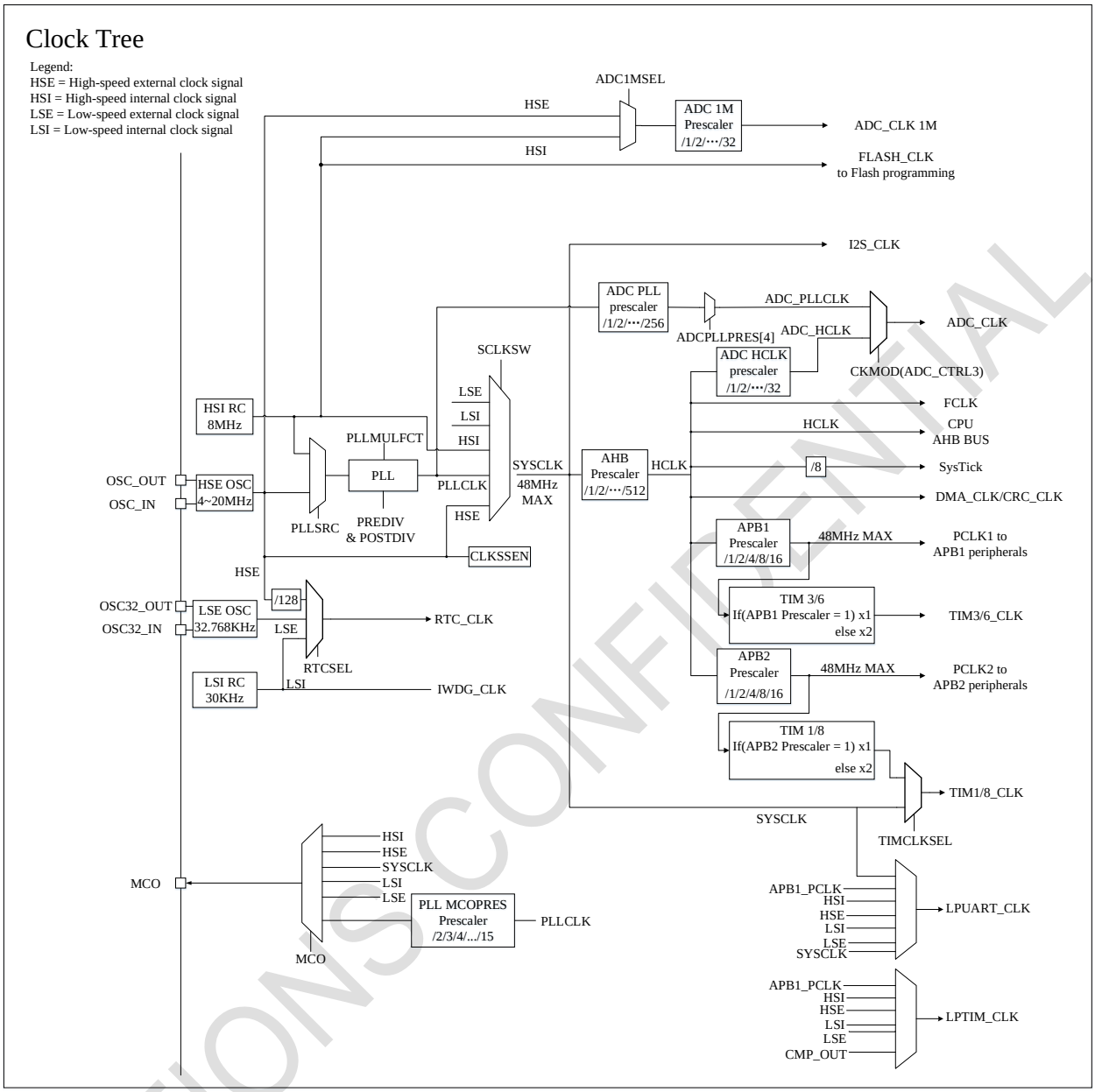
Figure 2-2 Clock Tree



2.5 Boot modes

At startup, BOOT0 pin and nBOOT0, nBOOT1 and nSWBOOT0_SEL option bits are used to select one of three boot options:

- Boot from main flash memory (default)
- Boot from system memory
- Boot from on-chip SRAM

The boot loader is located in the internal boot memory (system memory). It is used to reprogram the Flash memory by using USART1 (PA9 and PA10).

2.6 Power supply scheme

- VDD area: The voltage input range is 1.8V~5.5V, which mainly provides power input for Main Regulator, IO

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and clock reset system.

- VDDA area: The input voltage range is 1.8V~5.5V, which supplies power for most analog peripherals. For more information, please refer to the electrical characteristics section of the relevant data manual.
- VDDD area: The voltage regulator supplies power for the CPU, AHB, APB, SRAM, FLASH and most digital peripheral interfaces.
- PWR is the power control module of the entire device, its main function is to control N32G031 to enter different power modes and can be awakened by other events or interrupts. N32G031 supports RUN, LPRUN, SLEEP, STOP and PD modes.

2.7 Programmable voltage monitor

The power-on reset (POR) and power-down reset (PDR) circuits are integrated internally. This part of the circuit is always in working condition to ensure that the system works normally when the power supply voltage exceeds 1.8V. When VDD is lower than the set threshold (VPOR/PDR), the device remains in the reset state. The device has a programmable voltage monitor (PVD), which monitors the VDD/VDDA power supply and compares it with the threshold VPVD. When VDD is lower or higher than the threshold VPVD, it will generate an interrupt. The PVD function is turned on by software.

Table 4-6 is the value reference of VPOR/PDR and VPVD.

2.8 Low power mode

N32G031 is in operation mode after system reset or power-on reset. When the CPU does not need to run, you can choose to enter a low-power mode to save power.

N32G031 has the following four low-power modes:

- LPRUN mode (operation mode, the system is in 32.768KHz low-frequency and low-power operation mode)
- SLEEP mode (the core is stopped, all peripherals including Cortex®-M0 core peripherals (such as NVIC, SysTick) are still running)
- STOP mode (most of the clocks are turned off, the voltage regulator is still running in low power consumption mode)
- PD mode (VDDD power-down mode, VDD hold, 3 WAKEUP IO and NRST can wake up)
- In addition, the following methods can also reduce the power consumption in RUN mode:
  - Reduce the system clock frequency
  - Turn off the unused peripheral clocks on the APB and AHB buses
  - Optional configuration of PWR_CTRL4.STBFLH in RUN mode allows FLASH to enter deep standby mode. When exiting, the system needs to wait about 10us before re-accessing FLASH

2.9 DMA

Integrated 1 general purpose 5-channel DMA controller to manage memory-to-memory, peripheral-to-memory, and memory-to-peripheral data transfer;Each channel has a dedicated hardware DMA request logic, and each channel can be triggered by the software.The length of transmission of each channel, the source address and the destination address of transmission can be set separately by software.

DMA can be used for the main peripherals: SPI, I^2C, USART, Universal, Basic and Advanced Control Timers TIMX, I^2S, ADC.

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2.10 Real time clock (RTC)

Real Time Clock (RTC) has a set of BCD timers/counters that independently count continuously.Under the corresponding software configuration, the function of calendar can be provided.The RTC also provides two programmable alarm clock interrupts.

Two 32-bit registers contain decimal format (BCD) for subseconds, seconds, minutes, hours (in 12 or 24 hour format), days of the week, days (date), months, and years.

Subsecond values are provided in binary format as separate 32-bit registers.Additional 32-bit registers contain programmable seconds, minutes, hours, days of the week, days, months, and years.

The RTC provides automatic wake up in low power mode.

When a timestamp function event or intrusion detection event is enabled on GPIO, the current calendar is saved in a register.

2.11 Timer and watch dog

N32G031 supports 2 advanced-control timers, 1 general-purpose timer, 1 basic timer and 1 low-power timer, as well as 2 watchdog timers and 1 system tick timer.

The following table compares the functions of advanced-control timers, general-purpose timers, low-power timer and basic timers:

Table 2-1 Timer function comparison

Timer	Counter resolution	Counter type	Prescaler	Generate DMA request	Capture/Compare channel	Complementary output
TIM1 TIM8	16-bit	Up Down Up/Down	Any integer between 1~65536	support	4	support
TIM3	16-bit	Up Down Up/Down	Any integer between 1~65536	support	4	Unsupported
LPTIM	16-bit	Up	1/2/4/8/16/32/64/128	Unsupported	2	Unsupported
TIM6	16-bit	Up	Any integer between 1~65536	support	0	Unsupported

2.11.1 Basic timer TIM6

The basic timer (TIM6) contains a 16-bit auto-load counter, driven by a programmable prescaler. Can provide a time base for general-purpose timers.

- The main functions of the basic timer are as follows:
  - 16-bit automatic reload accumulating counter;
  - 16-bit programmable (can be modified in real time) prescaler, used to divide the input clock by a coefficient between 1 and 65536;
  - An interrupt/DMA request is generated when an update event (counter overflow) occurs

2.11.2 General purpose timer (TIM3)

Built-in a general-purpose timer (TIM3) that can run synchronously. This timer has a 16-bit auto-loading up/down counter, a 16-bit prescaler and 4 independent channels. Each channel can be used for input capture (for measuring pulse width), output comparison, PWM and single pulse mode output.

- The main functions of the general-purpose timer include:

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- 16-bit up, down, up/down automatic loading counter
- 16-bit programmable (can be modified in real time) prescaler, the frequency division coefficient of the counter clock frequency is any value between 1 and 65536
- 4 independent channels:
  - Input capture
  - Output comparison
  - PWM generation (edge or center alignment mode)
  - Single pulse mode output
- Use external signals to control the timer or the synchronization circuit when multiple timers are interconnected
- Interrupt/DMA is generated when the following events occur:
  - Update: counter overflow/downflow, counter initialization (through software or internal/external trigger)
  - Trigger events (counter start, stop, initialization or count by internal/external trigger)
  - Input capture
  - Output comparison
- Supports incremental (quadrature) encoder and Hall sensor circuits for positioning
- Trigger input as an external clock or current management by cycle

2.11.3 Low power timer (LPTIM)

LPTIM is a 16-bit timer that can work with extremely low power consumption. Thanks to the diversity of clock sources, LPTIM can operate in all power modes except PD mode. Since LPTIM can run without an internal clock source, it can be used as a "pulse counter", which is very useful in some applications. In addition, LPTIM has the ability to wake up the system from low-power consumption mode, which makes it suitable for implementing "timeout function" monitoring with extremely low power consumption.

LPTIM introduces a flexible clock scheme that provides the required functions and performance while minimizing power consumption.

- The main functions of low-power timers include:
  - 16-bit upward automatic loading counter
  - 3-bit prescaler, 8 kinds of frequency division factors (1, 2, 4, 8, 16, 32, 64, 128)
  - Abundant clock sources:
    - Internal clock sources: HSI, HSE, LSI, LSE, APB1 and CMP_OUT six clock sources
    - External clock source input through LPTIM (no LP oscillator runs during work, used for pulse counter applications)
  - 16-bit ARR automatic loading register
  - 16-bit comparator register
  - Continuous or single trigger mode
  - Optional software and hardware input trigger
  - Programmable digital anti-shake filter
  - Single pulse or PWM output can be configured
  - IO level polarity can be configured
  - Support encoder mode

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2.11.4 Advanced-control timer (TIM1/TIM8)

Two independent advanced timers (TIM1/TIM8), each timer is composed of a 16-bit auto-loading counter driven by a programmable prescaler. Supports multiple functions, including measuring the pulse width of the input signal (input capture), or generating output waveforms (output comparison, PWM, complementary PWM output embedded in dead time, etc.). Using timer prescaler and RCC clock control prescaler, the pulse width and waveform period can be adjusted from several microseconds to several milliseconds. Each timer is completely independent and does not share any resources with each other.

- The main functions of the advanced timer include:
  - 16-bit up, down, up/down automatic loading counter
  - 16-bit programmable (can be modified in real time) prescaler, the frequency division coefficient of the counter clock frequency is any value between 1 and 65536
  - Support up to 48Mhz as the timer input clock
  - Up to 4 independent channels:
    - Input capture
    - Output comparison
    - PWM generation (edge or center alignment mode)
    - Single pulse mode output
  - PWM trigger ADC sampling:
  - The trigger time point can be configured by software during the entire PWM cycle
  - Complementary output with programmable dead time
  - Use external signals to control the timer or the synchronization circuit when multiple timers are interconnected
  - Allow to update the repeat counter of the timer register after a specified number of counter cycles
  - Break input signal can put the timer output signal in a reset state or a known state
  - Interrupt/DMA is generated when the following events occur:
    - Update: counter overflow/downflow, counter initialization (through software or internal/external trigger)
    - Trigger events (counter start, stop, initialization or count by internal/external trigger)
    - Input capture
    - Output comparison
    - Break signal input
  - Supports incremental (quadrature) encoder and Hall sensor circuits for positioning
  - Trigger input as an external clock or current management by cycle

In debug mode, the counter can be frozen and the PWM outputs are disabled, thereby cutting off the switches controlled by these outputs.

2.11.5 Systick

This timer is specific to the real-time operating system and can also be used as a standard decrement counter.

- It has the following characteristics:
  - 24-bit decrement counter
  - Automatic reload function

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- A maskable system interrupt can be generated when the counter is 0
- programmable clock source

2.11.6 Watchdog timer WDG

Two watchdogs are supported, Independent Watchdog (IWDG) and Window Watchdog (WWDG).Two watchdogs provide increased security, timing accuracy and flexibility in use.

Independent watchdog (IWDG)

The independent watchdog is based on a 12-bit decline counter and an 8-bit pre-divider, driven by a standalone low-speed RC oscillator that remains effective in the event of a master clock failure and operates in STOP mode.Once activated, IWDG generates a reset when the counter counts to 0x000 if the dog is not fed within the set time (clearing the watchdog counter). It can be used to reset the entire system in the event of an application problem, or as a free timer to provide timeout management for the application.The option byte can be configured to be software or hardware enabled watchdog.Reset and low power wake-up are available.

Window watchdog (WWDG)

Window watchdogs are usually used to monitor software failures caused by external interference or unforeseen logic conditions that cause the application to deviate from the normal operating sequence. Unless the value of the down counter is refreshed before the T6 bit becomes 0, the watchdog circuit will generate an MCU reset when the preset time period is reached. Before the down counter reaches the window register value, if the 7-bit down counter value (in the control register) is refreshed, an MCU reset will also be generated. This indicates that the down counter needs to be refreshed in a limited time window.

- Main features:
  - WWDG is driven by the clock after the APB1 clock is divided
  - Programmable free running decrement counter
  - Conditional reset
  - When the decrement counter value is less than 0x40, (if the watchdog is started) a reset is generated
  - Reset when the decrement counter is reloaded outside the window (if the watchdog is activated)
  - If the watchdog is enabled and interrupts are allowed, an early wake-up interrupt (EWI) is generated when the decrements counter equals 0x40, which can be used to reload the counter to avoid a WWDG reset

2.12 Inter-integrated circuit (I2C)

Two independent I2C bus interfaces that provide multi-host functionality to control all I2C bus specific timing, protocol, mediation, and timing.Supports multiple communication rate modes (up to 1MHz), supports DMA operation, and is compatible with SMBUS 2.0.The I2C module has a variety of uses, including CRC code generation and verification, SMBUS (System Management Bus) and PMBUS (Power Management Bus).

- The main functions of I2C interface are described as follows:
  - Multi-host function: the module can be used as a master device or a slave device
  - I2C main equipment functions:
    - Generate clock
    - Generate start and stop signals
  - I2C slave device features:
    - Programmable address detection
    - The I^2C interface supports 7-bit or 10-bit addressing, and supports dual slave address response in 7-bit slave mode

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- Stop bit detection

- Generate and detect 7-bit / 10-bit addresses and broadcast calls
- Support different communication speeds:
  - Standard speed (up to 100 kHz)
  - Fast (up to 400 kHz)
  - Fast + (up to 1MHz)
- Status flag:
  - Transmitter/receiver mode flag
  - Byte send end flag
  - I^2C bus busy sign
- Error flag:
  - Arbitration lost in the main mode
  - Response (ACK) error after address/data transmission
  - Misaligned start or stop conditions detected
  - Prohibit overflowing or underflowing when elongating the clock function
- 2 interrupt vectors:
  - 1 interrupt for address/data communication successful
  - 1 interrupt for error
- Optional elongated clock feature
- DMA with a single byte cache
- Generate or verify configurable PEC(packet error detection):
  - The PEC value in send mode can be transmitted as the last byte
  - A PEC error check for the last received byte
- SMBus 2.0 compatible:
  - Low timeout delay for 25 ms clock
  - 10 ms master device cumulative clock low expansion time
  - 25 ms accumulates low expansion time from the device clock
  - Hardware PEC generation/verification with ACK control
  - Support for address resolution protocol (ARP)
- Compatible with the SMBus

2.13 Universal synchronous asynchronous receiver transmitter (USART)

In the N32G031 series, three serial transceiver interfaces are integrated, including two universal synchronous/asynchronous transceivers (USART1, USART2) and one universal asynchronous transceiver (LPUART) supporting low power mode operation.These three interfaces provide synchronous/asynchronous communication, support for IRDA SIR ENDEC transport codec, multi-processor communication mode, single-wire semi-duplex communication mode, and LIN master/slave functionality.

The USART1 and USART2 interfaces have hardware CTS and RTS signal management, ISO7816 compatible smart card mode and SPI-like communication mode, all interfaces can use DMA operation.

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- The main features of USART are as follows:
  - Full-duplex, asynchronous communication
  - NRZ standard format
  - Fractional baud rate generator system, baud rate programmable for sending and receiving up to 3Mbits/s
  - Programmable data word length (8 or 9 bits)
  - Configurable stop bits, supporting 1 or 2 stop bits
  - The ability of LIN to send a synchronous break and LIN to detect a slave break. When the USART hardware is configured to LIN, the 13-bit break is generated and the 10/11 bit break is detected
  - Output sending clock for step transmission
  - IRDA SIR encoder decoder, supports 3/16 bit duration in normal mode
  - Smart card simulation function:
    - The smart card interface supports the asynchronous smart card protocol defined in ISO7816-3 standard
    - 0.5 and 1.5 stop bits for smart cards
  - Single-wire half-duplex communication
  - Conconfigurable multi-buffer communication using DMA, receiving/sending bytes in SRAM using a centralized DMA buffer
  - Separate transmitter and receiver enabling bits
  - Detection mark
    - Receive buffer full
    - Send buffer empty
    - End of transmission flag
  - Check control
    - Send check bit
    - Check the received data
  - Four error detection flags
    - Overflow error
    - Noise error
    - Frame error
    - Check error
  - 10 USART interrupt sources with flags
    - CTS change
    - LIN break character detection
    - The send data register is empty
    - Send complete
    - Receive data register full
    - The bus is detected to be idle
    - Overflow error
    - Frame error

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- Noise error
- Check error

- Multi-processor communication, if the address does not match, then into the silent mode;
- Wake up from silent mode (by idle bus detection or address flag detection)
- There are two ways to wake up the receiver: address bit (MSB, bit 9), and bus idle
- Mode configuration

USART modes	USART1	USART2	LPUART
Asynchronous mode	support	support	support
Hardware flow control	support	support	nonsupport
Multi-cache Communication (DMA)	support	support	support
Multiprocessor communication	support	support	support
Synchronous	support	support	nonsupport
Smart card	support	support	nonsupport
Half duplex (single wire mode)	support	support	support
IrDA	support	support	support
LIN	support	support	support

2.14 Serial Peripheral interface (SPI)

Support 2 SPI interfaces, SPI allows the chip to communicate with external devices in half/full duplex, synchronous, serial mode.This interface can be configured to be in master mode and provide a communication clock (SCK) for external slave devices.The interface can also work in a multi-master configuration.It can be used for a variety of purposes, including dual wire simplex synchronous transmission using a two-way data line, and reliable communication using CRC calibration.

- The main functions of the SPI interface are as follows:
  - Full-duplex synchronous transmission
  - Double wire simplex synchronous transmission with or without a third two-way data line
  - 8 or 16 bit transmission frame format selection
  - Support master mode or slave mode
  - Support multi-master mode
  - Fast communication between master mode and slave mode
  - NSS can be managed by software or hardware in both master mode and slave mode: dynamic change of master/slave operation mode
  - Programmable clock polarity and phase
  - Programmable data order, MSB before or LSB before
  - Dedicated send and receive flags that trigger interrupts
  - SPI bus busy status flag
  - Hardware CRC to support reliable communication:
    - In send mode, the CRC value can be sent as the last byte
    - In full duplex mode, CRC check is automatically carried out on the last byte received
  - Main mode failures, overloads, and CRC error flags that trigger interrupts
  - Single-byte send and receive buffers that support DMA functionality: Generates send and receive requests

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- Maximum interface speed: 18Mbps

2.15 Integrated Interchip Sound (I2S)

I2S is a 3-pin synchronous serial interface communication protocol that can operate in master or slave mode. It can be configured for 16-bit, 24-bit, or 32-bit transmission, as well as input or output channels, and supports audio sampling frequencies from 8kHz to 96kHz.It supports four audio standards, including the Philips I2S standard, the MSB and LSB alignment standard, and the PCM standard.

It can work in both master and slave modes in half duplex communication.When it is the master device, it provides a clock signal to an external slave device through the interface.

- The main functions of I^2S interface are as follows;
  - Half-duplex communication (only send or receive at the same time);
  - Master or slave operation;
  - 8-bit linear programmable pre-divider for accurate audio sampling frequency (8kHz to 96kHz);
  - The data format can be 16-bit, 24-bit, or 32-bit;
  - Audio channel fixed packet frame is 16 bit (16 bit data frame) or 32 bit (16, 24 or 32 bit data frame);
  - Programmable clock polarity (stable state);
  - Overflow flag bits in send mode and overflow flag bits in master/slave receive mode;
  - 16-bit data registers are used for sending and receiving, with one register at each end of the channel;
  - Supported I^2S protocols:
    - I^2S Philips standard;
    - MSB alignment standard (left alignment);
    - LSB alignment standard (right alignment);
    - PCM standard (16-bit channel frames with long or short frame synchronization or 16-bit data frames extended to 32-bit channel frames);
  - Data direction is always MSB first;
  - Both sending and receiving have DMA capability;
  - The master clock can be output to external audio devices, fixed frequency is 256xFS(FS is the audio sampling frequency);

2.16 General-purpose input/outputs (GPIOs)

GPIO (General Purpose Input/Output) stands for Generic I/O, AFIO (Alternate-Function Input/Output) stands for Multiuse Function I/O.The chip supports up to 40 GPIOs and is divided into 4 groups (GPIOA/GPIOB/GPIOC/ GPIOF), group A/B has 16 ports per group, group C has 3 ports and group F has 5 ports.GPIO ports share pins with other reusable peripherals, and users can configure them flexibly according to their needs.Each GPIO pin can be independently configured as an output, input, or multiplexed peripheral function port.Except for analog input pins, all other GPIO pins have high current flow capability.

- The main characteristics of GPIO are described as follows:
  - GPIO ports can be configured separately by the software in the following modes:
    - Input floated
    - Input pull-up
    - Input dropdown
    - Simulation function

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- Open drain output and up/down can be configured
- Push-pull output and up/down configurable
- Push-pull multiplexing function and up/down configurable
- Open drain multiplexing function and up/down configurable

- Separate bit setting or bit clearing
- All IO support external interrupt functionality
- All IO support low-power mode wake-up, with rising or falling edges configurable
- Sixteen extis can be used for SLEEP or STOP mode wake up, and all I/O can be reused as EXTI
- PA0/PC13/PA2 three wake-up IO can be used for PD mode wake-up, I/O filtering time is 1us maximum
- Supports software remap I/O reuse
- Support GPIO locking mechanism, reset mode to clear the locked state

Each I/O port bit can be programmed arbitrarily, but the I/O port register must be accessed as a 32-bit word (16-bit halfword or 8-bit byte access is not allowed).

2.17 Analog to digital converter (ADC)

12-bit ADC is a high-speed successive approximation analog-to-digital converter. It has up to 15 channels and can measure 12 external and 3 internal signal sources. The A/D conversion of each channel can be executed in single, continuous, scanning or discontinuous mode. The ADC result can be left-aligned or right-aligned stored in the 16-bit data register; ADC input clock must not exceed 18MHz.

- The main characteristics of ADC are described as follows:
  - Support 1 ADC, single-ended input, can measure 12 external and 4 internal signal sources
  - Support 12-bit resolution, the highest sampling rate is 1MSPS
  - ADC clock source is divided into working clock source, sampling clock source and timing clock source
    - Only AHB_CLK can be configured as a working clock source, up to 48MHz
    - PLL can be configured as a sampling clock source, up to 18MHz, support frequency division 1, 2, 4, 6, 8, 10, 12, 16, 32, 64, 128, 256
    - AHB_CLK can be configured as the sampling clock source, up to 18MHz, support frequency division 1, 2, 4, 6, 8, 10, 12, 16, 32
    - The timing clock is used for internal timing functions, and the frequency must be configured to 1MHz
  - Support timer trigger ADC sampling
  - Interrupts are generated at the end of conversion, the end of injection conversion, and the occurrence of analog watchdog events
  - Single and continuous conversion mode
  - Auto scan mode from channel 0 to channel N
  - Data alignment with embedded data consistency
  - Sampling interval can be programmed separately per channel
  - Both rule conversion and injection conversion have external trigger options
  - discontinuous mode
  - ADC power supply requirements: 2.4V to 5.5V
  - ADC input range: $0 \leq VIN \leq VDDA$
  - During regular channel conversion, a DMA request is generated.

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2.18 Operational Amplifier (OPAMP)

Built-in an independent operational amplifier with multiple working modes such as external amplification, internal follower and programmable amplifier (PGA) (or both internal amplification and external filtering).

- The main functions are as follows:
  - Support rail-to-rail input
  - OPA linear output range 0.4V~VDDA-0.4V
  - Can be configured as independent op amp and programmable gain opamp
  - Forward and reverse input multiple selection
  - OPAMP working mode can be configured as:
    - Independent mode (external gain setting)
    - PGA mode, programmable gain is set to 2X, 4X, 8X, 16X, 32X
    - Follower mode
  - The internally connected ADC channel is used to measure the output signal of the operational amplifier

2.19 Analog comparator (COMP)

Built-in 1 comparator, which can be used as a separate device (all ports of the comparator are led to I/O), or it can be used in combination with a timer. In motor control applications, it can be used in conjunction with the PWM output from the timer to form a cycle-by-cycle Current control.

- The main functions of the comparator are as follows:
  - 1 independent comparator COMP, and it is a low-power comparator (can work in LPRUN, SLEEP and STOP modes)
  - Built-in a 64-level programmable reference input voltage source VREF
  - Support filter clock, filter reset
  - Output polarity can be configured high and low
  - Hysteresis configuration can be configured without, low, medium, high
  - The comparing results can be output to the I/O port or trigger the timer for capturing events, OCREF_CLR events, braking events, and generating interrupts
  - Input channel can be multi-selected I/O port, VREF
  - It can be equipped with read-only or read-write, and it needs to be reset to unlock when locked
  - Support blanking (Blanking), the blanking source can be configured to generate Blanking
  - COMP can wake up the system from low power consumption mode by generating an interrupt, and COMP has the ability to wake up the system from STOP
  - Configurable filter window size
  - Configurable filter threshold size
  - Configurable sampling frequency for filtering

2.20 Temperature Sensor (TS)

The temperature sensor generates a voltage that changes linearly with temperature, and the conversion range is between 1.8V <VDDA <5.5V. The temperature sensor is internally connected to the input channel of ADC_IN12 to convert the output of the sensor to a digital value.

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2.21 BEEPER

The BEEPER module supports complementary outputs and can generate periodic signals to drive external passive beeper. Used to generate prompt sound or alarm sound.

2.22 HDIV/SQRT

The divider (HDIV) and square root (SQRT) are mainly used in some scenarios with high requirements for computing energy efficiency, and are used to partially supplement the deficiencies of the microcontroller in computing. The divider and square root calculator can perform division or square root calculation of unsigned 32-bit integers.

- The main features of HDIV and SQRT are as follows:
  - Only support word operation
  - 8 clock cycles to complete an unsigned integer division operation
  - 32-bit dividend, 32-bit divisor, output 32-bit quotient and 32-bit remainder
  - Divisor is zero warning flag, division operation end flag
  - 32-bit unsigned square root integer, 16-bit root root output
  - Complete an unsigned integer square root operation in 8 clock cycles
  - You can judge whether the calculation is complete by setting the interrupt enable or query the relevant register bits

2.23 Cyclic Redundancy Check Calculation Unit (CRC)

Integrating CRC32 and CRC16 functions, the cyclic redundancy check (CRC) calculation unit obtains any CRC calculation result according to a fixed generator polynomial. In many applications, CRC-based technology is used to verify the consistency of data transmission or storage. Within the scope of the EN/IEC 60335-1 standard, it provides a means to detect flash memory errors. The CRC calculation unit can be used to calculate the signature of the software in real time and compare it with the signature generated when the software is linked and generated

- The main characteristics of CRC are as follows:
  - CRC16: Support polynomial $X^{16}+X^{15}+X^{2}+X^{0}$
  - CRC32: Support polynomial $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^{8} + X^{7} + X^{5} + X^{4} + X^{2} + X +1$
  - CRC calculation time: 4 AHB clock cycles (HCLK)
  - The initial value of cyclic redundancy calculation can be configured
  - Support DMA mode

2.24 Unique device ID (UID)

N32G031 series products have built-in two unique device ID of different lengths, 96-bit UID (Unique device ID) and 128-bit UCID (Unique Customer ID). These two device serial numbers are stored in the system configuration block of the flash memory. The information contained in them is programmed at the factory, and is guaranteed to be unique to any microcontroller of the N32G031 series under any circumstances. User applications or external devices can be read through the CPU or SWD interface and cannot be modified.

The UID is 96 bits, usually used as a serial number or as a password. When programming the flash memory, this unique identification is combined with the software encryption and decryption algorithm to further improve the security of the code in the flash memory. It can also be used for activation with security Functional bootloader (Secure Bootloader).

The UCID is 128 bits and complies with the definition of the national technology chip serial number. It contains

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information about chip production and version.

The UCID is 128 bits and complies with the definition of the chip serial number of Nations Technologies Inc. It contains information about chip production and version.

2.25 Serial wire SWD debug port (SWD)

The Arm® SWD Interface is embedded.

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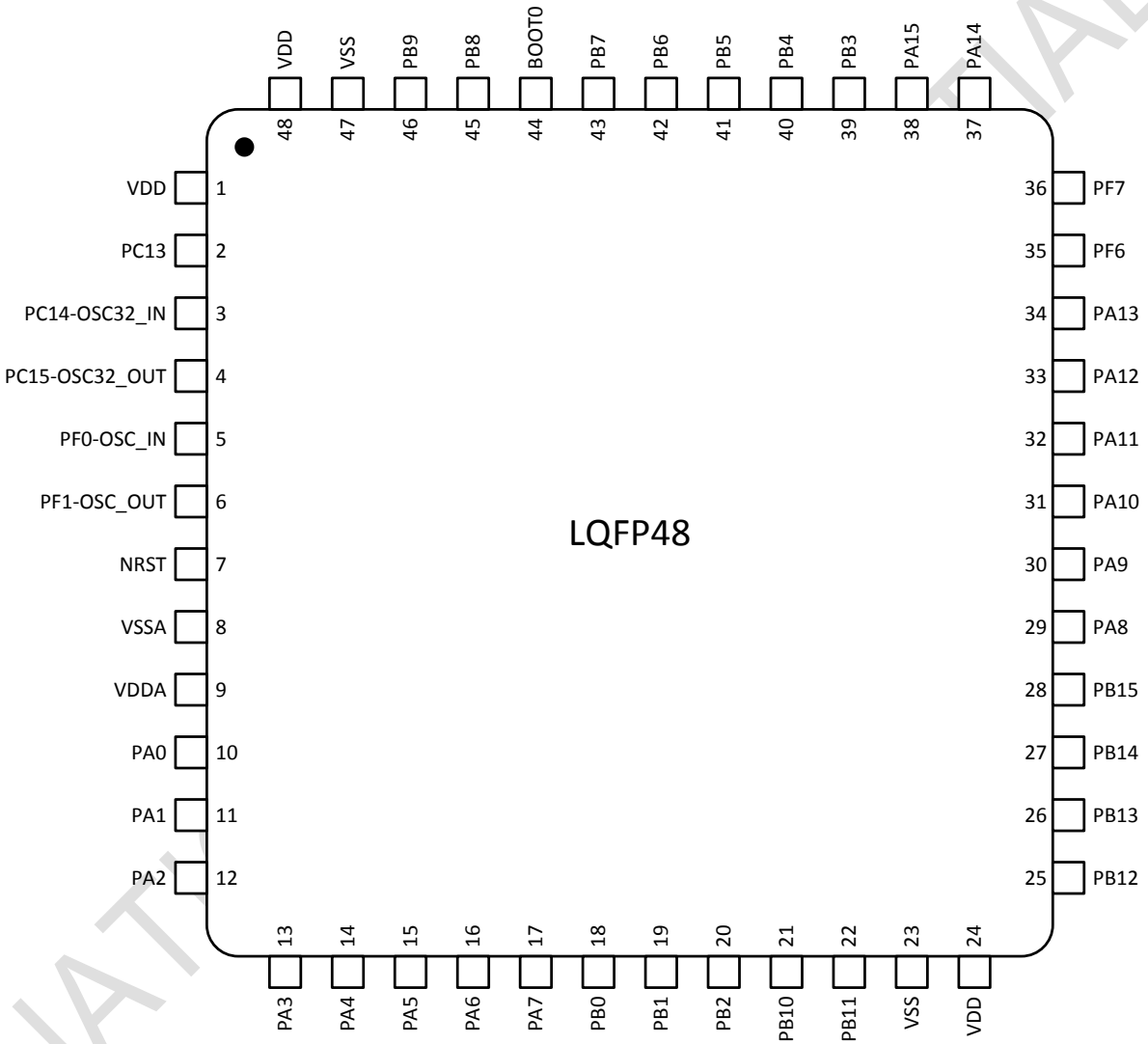
3 Pin descriptions

3.1 Package

3.1.1 LQFP48

Figure 3-1 N32G031 Series LQFP48 pinouts



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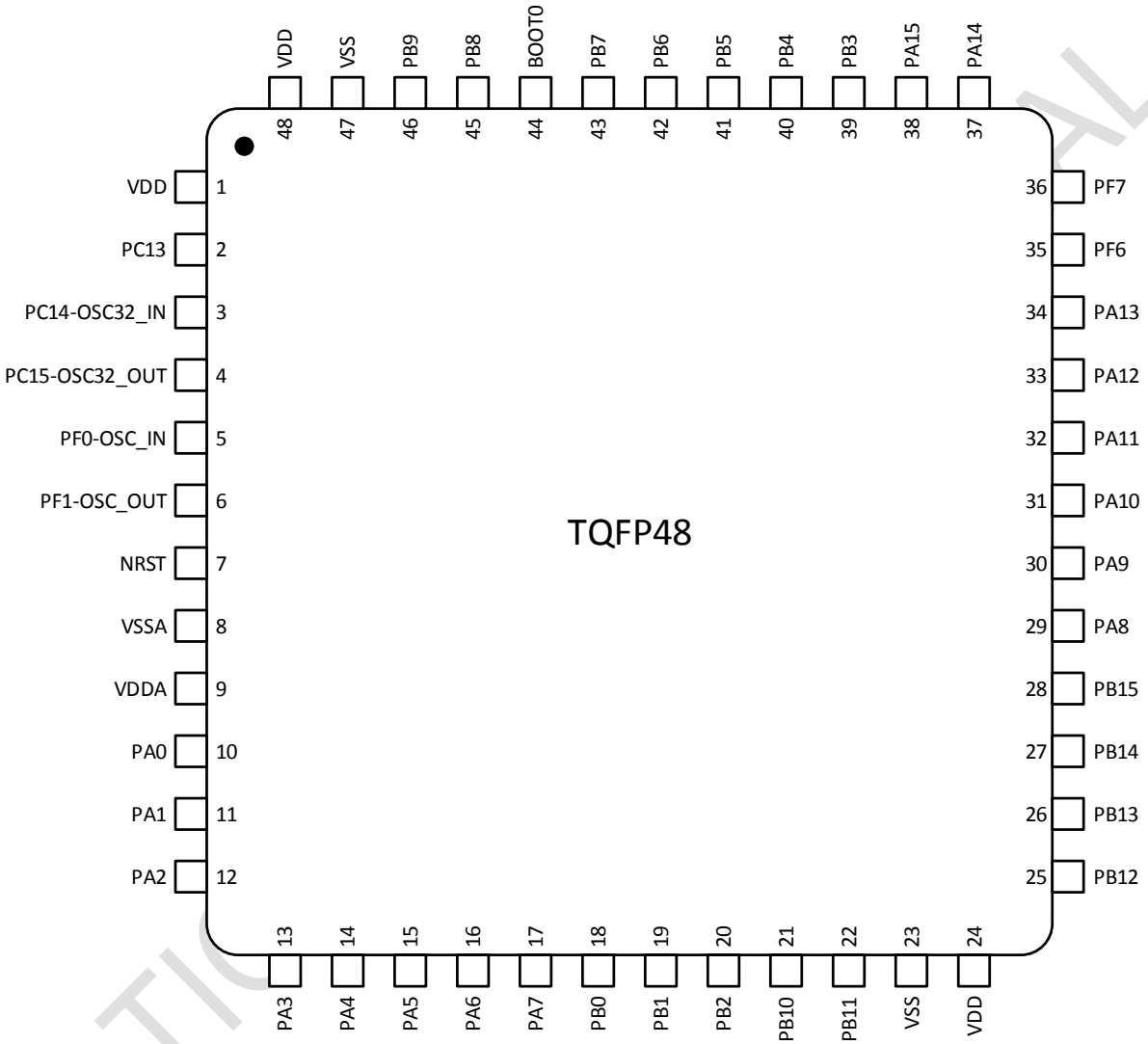
3.1.2 TQFP48

Figure 3-2 N32G031 Series TQFP48 pinouts



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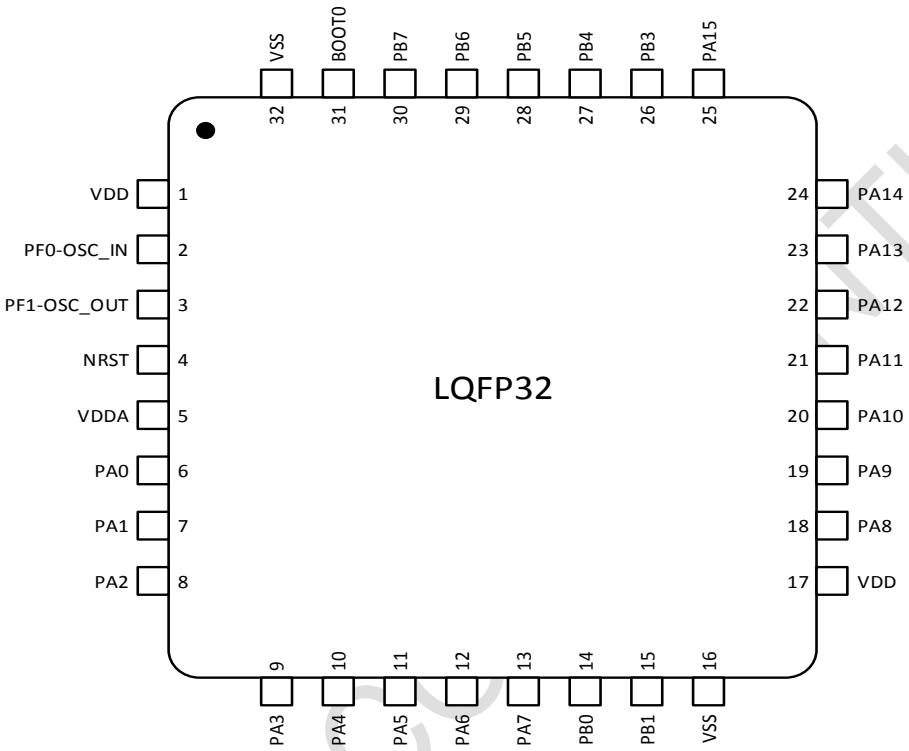
3.1.3 LQFP32

Figure 3-3 N32G031 Series LQFP32 pinouts



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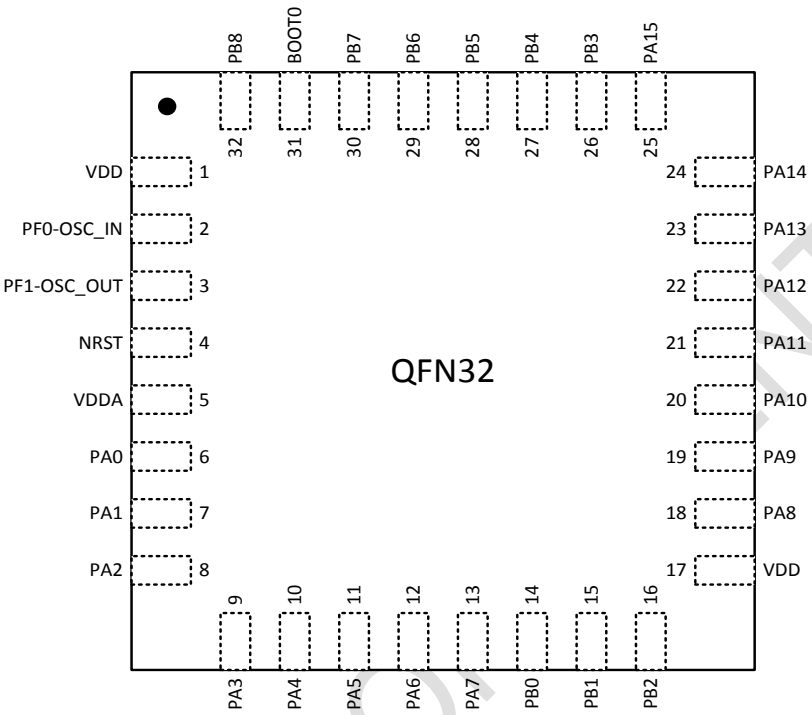
3.1.4 QFN32 (5mx5m)

Figure 3-4 N32G031 Series QFN32 (5mx5m) pinouts



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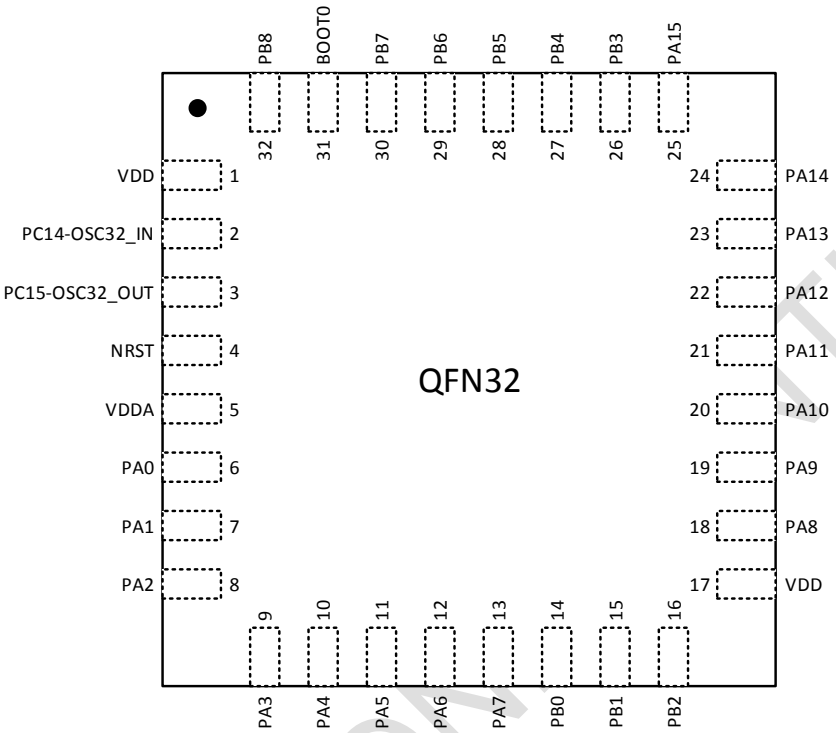
3.1.5 QFN32 (4mx4m)

Figure 3-5 N32G031 Series QFN32 (4mx4m) pinouts



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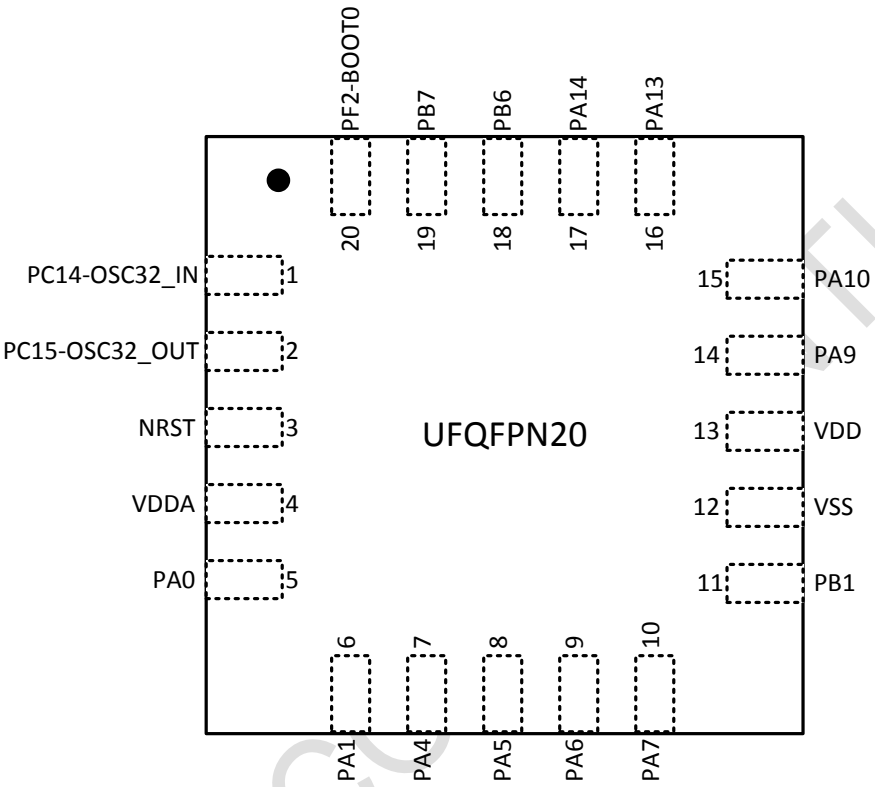
3.1.6 UFQFPN20

Figure 3-6 N32G031 Series UFQFPN20 pinouts



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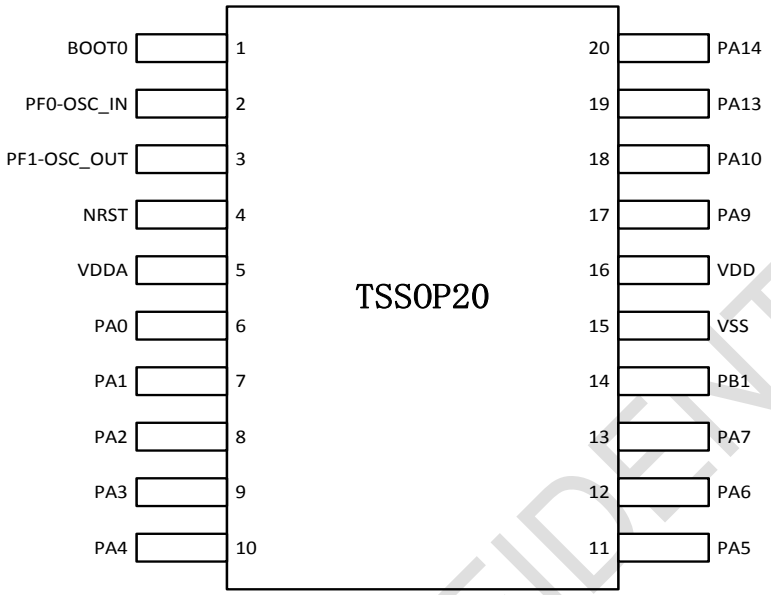
3.1.7 TSSOP20

Figure 3-7 N32G031 Series TSSOP20 pinouts



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3.2 Pin definitions

Table 3-1 Pin definitions

Package						Pin name (function after reset)	Type(1)	I/O structure	Alternate functions	Additional functions
LQFP48	LQFP32	QFN32(5mx5m)	QFN32(4mx4m)	UFQFPN20	TSSOP20					
1	1	1	1	-	-	VDD	S	-	Complementary power supply	
2	-	-	-	-	-	PC13	I/O	TC	RTC_TAMP1, RTC_TS, RTC_OUT,	WKUP1
3	-	-	2	1	-	PC14-OSC32_IN (PC14)	I/O	TC	-	OSC32_IN
4	-	-	3	2	-	PC15-OSC32_OUT (PC15)	I/O	TC	-	OSC32_OUT
5	2	2	-	-	2	PF0-OSC_IN (PF0)	I/O	TC	I2C1_SDA	OSC_IN, OPAMP_VINP
6	3	3	-	-	3	PF1-OSC_OUT (PF1)	I/O	TC	I2C1_SCL, USART1_CK, USART2_CK	OSC_OUT
7	4	4	4	3	4	NRST	I	RST	Device reset input / internal reset output (active low)	
8	-	-	-	-	-	VSSA	S	-	Analog ground	
9	5	5	5	4	5	VDDA	S	-	Analog power supply	
10	6	6	6	5	6	PA0	I/O	TC	USART1_CTS USART2_CTS LPUART_TX, SPI1_SCK, I2S_CK USART2_RX, LPTIM_IN1, TIM8_CH1, TIM8_ETR, LPUART_RX,	ADC_IN0, RTC_TAMP2, WKUP0, COMP_INM, COMP_OUT, OPAMP_VINP
11	7	7	7	6	7	PA1	I/O	TC	USART1_RTS USART2_RTS, EVENTOUT, SPI1_NSS, I2S_WS, LPTIM_IN2, TIM8_CH2, I2C1_SMBA, TIM3_ETR, LPUART_TX	ADC_IN1, COMP_INP, OPAMP_VINP

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12	8	8	8	-	8	PA2	I/O	TC	USART1_TX, USART2_TX, TIM8_CH3, SPI1_MOSI, I2S_SD, TIM1_BKIN	ADC_IN2, WKUP2, OPAMP_VINM
13	9	9	9	-	9	PA3	I/O	TC	USART1_RX, USART2_RX, TIM8_CH4, TIM1_CH2, SPI1_MISO, I2S_MCK, LPUART_TX	ADC_IN3, COMP_INP
14	10	10	10	7	10	PA4	I/O	TC	SPI1_MISO I2S_MCK, USART1_CK, USART2_CK, TIM3_CH1, TIM1_CH1, SPI1_NSS, I2S_WS, I2C1_SCL, TIM8_ETR, LPUART_TX	ADC_IN4, COMP_INM, OPAMP_VINP
15	11	11	11	8	11	PA5	I/O	TC	SPI1_SCK, I2S_CK, TIM8_ETR, TIM1_CH2N, TIM1_CH3 SPI1_MOSI, I2C_SD, TIM8_CH1	ADC_IN5, COMP_INM, OPAMP_VINM
16	12	12	12	9	12	PA6	I/O	TC	SPI1_MISO, TIM3_CH1, TIM1_BKIN, TIM8_CH1, EVENTOUT, LPUART_CTS, LPUART_TX, I2C2_SCL, LPTIM_ETR, BEEPER_OUT	ADC_IN6, COMP_OUT, OPAMP_VOUT
17	13	13	13	10	13	PA7	I/O	TC	SPI1_MOSI, SPI2_NSS, I2S_SD, TIM3_CH2, TIM1_CH1N, TIM8_CH2, EVENTOUT, LPUART_RX, I2C2_SDA, BEEPER_N_OUT, USART2_CTS,	ADC_IN7, OPAMP_VINP, COMP_INP
18	14	14	14	-	-	PB0	I/O	TC	TIM3_CH3, TIM1_CH2N, EVENTOUT, SPI2_SCK,	ADC_IN8, OPAMP_VINP

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19	15	15	15	11	14	PB1	I/O	TC	TIM3_CH3, TIM3_CH4, TIM1_CH3N, LPUART_RTS, I2S_SD SPI2_MOSI, USART2_CK, SPI1_MOSI,	ADC_IN9, OPAMP_VINM
20	-	16	16	-	-	PB2	I/O	TC	I2C1_SMBA, I2C2_SMBA, TIM3_CH4, LPTIM_OUT	ADC_IN10, OPAMP_VINM
21	-	-	-	-	-	PB10	I/O	TC	SPI2_SCK, I2C1_SCL, I2C2_SCL, LPUART_TX, TIM3_ETR, SPI1_MOSI, I2S_SD	ADC_IN11
22	-	-	-	-	-	PB11	I/O	TC	I2C1_SDA, I2C2_SDA, EVENTOUT, LPUART_RX, TIM8_CH3	-
23	16	-	-	12	-	VSS	S	-	Ground	
24	17	17	17	13	-	VDD	S	-	Digital power supply	
25	-	-	-	-	-	PB12	I/O	TC	SPI1_NSS, I2S_WS, SPI2_NSS, TIM1_BKIN, EVENTOUT, TIM8_CH1	-
26	-	-	-	-	-	PB13	I/O	TC	SPI1_SCK, I2S_CK, SPI2_SCK, I2C2_SCL, TIM1_CH1N, LPUART_CTS, TIM8_CH2	-
27	-	-	-	-	-	PB14	I/O	TC	SPI1_MISO, SPI2_MISO, I2C2_SDA, TIM1_CH2N, TIM8_CH3, LPUART_RTS	OPAMP_VINP
28	-	-	-	-	-	PB15	I/O	TC	SPI1_MOSI, I2S_SD, SPI2_MOSI, TIM1_CH3N, TIM8_CH3N, TIM8_CH4,	RTC_REFIN,

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29	18	18	18	-	-	PA8	I/O	TC	USART1_CK, TIM1_CH1, EVENTOUT, MCO, SPI2_NSS, TIM8_CH2N,	-
30	19	19	19	14	17	PA9	I/O	TC	USART1_TX, TIM1_CH2, TIM8_BKIN, I2C1_SCL, I2C2_SCL, SPI2_SCK, TIM8_CH1N, LPTIM_OUT, USART2_TX,	-
31	20	20	20	15	18	PA10	I/O	TC	USART1_RX, TIM1_CH3, TIM8_BKIN, I2C1_SDA, I2C2_SDA, SPI2_ MISO, USART2_RX, RTC_REFIN,	-
32	21	21	21	-	-	PA11	I/O	TC	USART1_CTS, TIM1_CH4, EVENTOUT, I2C2_SCL, SPI2_ MOSI	COMP_OUT
33	22	22	22	-	-	PA12	I/O	TC	USART1_RTS, TIM1_ETR, EVENTOUT, I2C2_SDA, SPI2_MISO,	COMP_OUT
34	23	23	23	16	19	PA13 (SWDIO)	I/O	TC	USART1_TX, SWDIO, USART1_RX, USART2_RX, I2C1_SDA, SPI1_SCK I2S_CK	-
35	-	-	-	-	-	PF6	I/O	TC	I2C1_SCL, I2C2_SCL, SPI2_SCK	-
36	-	-	-	-	-	PF7	I/O	TC	I2C1_SDA , I2C2_SDA , SPI2_NSS	-
37	24	24	24	17	20	PA14 (SWCLK)	I/O	TC	USART1_TX, USART2_TX, SWCLK, I2C1_SMBA, SPI1_MISO,	-
38	25	25	25	-	-	PA15	I/O	TC	SPI1_NSS, I2S_WS, USART1_RX, USART2_RX, LPUART_RTS, EVENTOUT	-

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39	26	26	26	-	-	PB3	I/O	TC	SPI1_SCK, I2S_CK, EVENTOUT, LPUART_TX, TIM3_ETR	-
40	27	27	27	-	-	PB4	I/O	TC	SPI1_MISO, TIM3_CH1, EVENTOUT, TIM8_BKIN, LPUART_RX, LPTIM_OUT	-
41	28	28	28	-	-	PB5	I/O	TC	SPI1_MOSI, I2S_SD, I2C1_SMBA, TIM8_BKIN, TIM3_CH2, LPUART_TX, LPTIM_IN1, TIM8_CH3N	-
42	29	29	29	18	-	PB6	I/O	TC	I2C1_SCL, USART1_TX, TIM8_CH1N, TIM8_CH3, LPTIM_ETR	-
43	30	30	30	19	-	PB7	I/O	TC	I2C1_SDA, USART1_RX, TIM8_CH2N, LPUART1_CTS, LPUART1_RX, LPTIM_IN2, TIM8_CH4,	-
44	31	31	31	20	1	PF2-BOOT0	I	B	Boot memory selection	
45	-	32	32	-	-	PB8	I/O	TC	I2C1_SCL, TIM8_CH1	-
46	-	-	-	-	-	PB9	I/O	TC	I2C1_SDA, USART1_TX, SPI2_NSS, TIM8_CH2, EVENTOUT	-
47	32	-	-	-	15	VSS	S	-	Ground	
48	-	-	-	-	16	VDD	S	-	Digital power supply	

1. *I = input, O = output, S = power, HiZ = High resistance, B = BOOT0 pin*
2. *TC: Standard 5V I/O, RST: bidirectional reset pin with built-in weak pull-up resistor*
3. *Some functions are only supported in some models of chips.*
4. *During and immediately after the reset, the multiplexing function is not enabled, and the I/O port is configured as an analog input mode (PMODEx[1:0]=2'b11). But there are a few exception signals:*
   - *NRST has no GPIO function by default*
   - *NRST pull-up input*
   - *After reset, the default state of the pins related to the debugging system is the SWD function, and the SWD pin is configured to input pull-up or pull-down mode:*
     - *PA14: SWCLK is configured as input pull-down mode*

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- *PA13: SWDIO is configured as input pull-up mode*

◆ *PF0:*

- *PF0 is configured as floating input mode by default*
- *PF0 is multiplexed to OSC_IN*

◆ *BOOT0:*

- *BOOT0 is configured as pull-down input mode by default*

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4 Electrical characteristics

4.1 Test conditions

All voltages are based on VSS unless otherwise specified.

4.1.1 Minimum and maximum values

Unless otherwise specified, 100% of the products are tested on the production line at an ambient temperature of TA=25℃ and TA=TAmax (TAmax matches the selected temperature range), and all the minimum and maximum values will be at the worst Guaranteed under the conditions of ambient temperature, supply voltage and clock frequency.

4.1.2 Typical values

Unless otherwise specified, typical data is based on TA=25°C and VDD=3.3V (1.8V ≤ VDD ≤ 5.5V voltage range). These data are only used for design guidance and not tested.

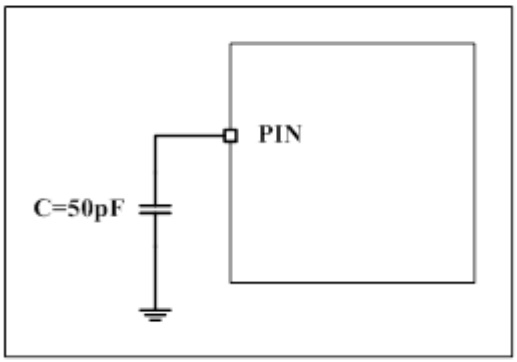
4.1.3 Typical curves

Unless otherwise specified, typical curves are for design guidance only and have not been tested.

4.1.4 Loading capacitor

The load conditions when measuring the pin parameters are shown in Figure 4-1.

Figure 4-1 pin loading conditions



4.1.5 Pin input voltage

The measurement method of the input voltage on the pin is shown in Figure 4-2.

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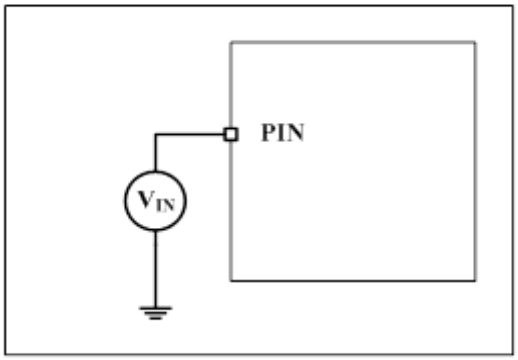
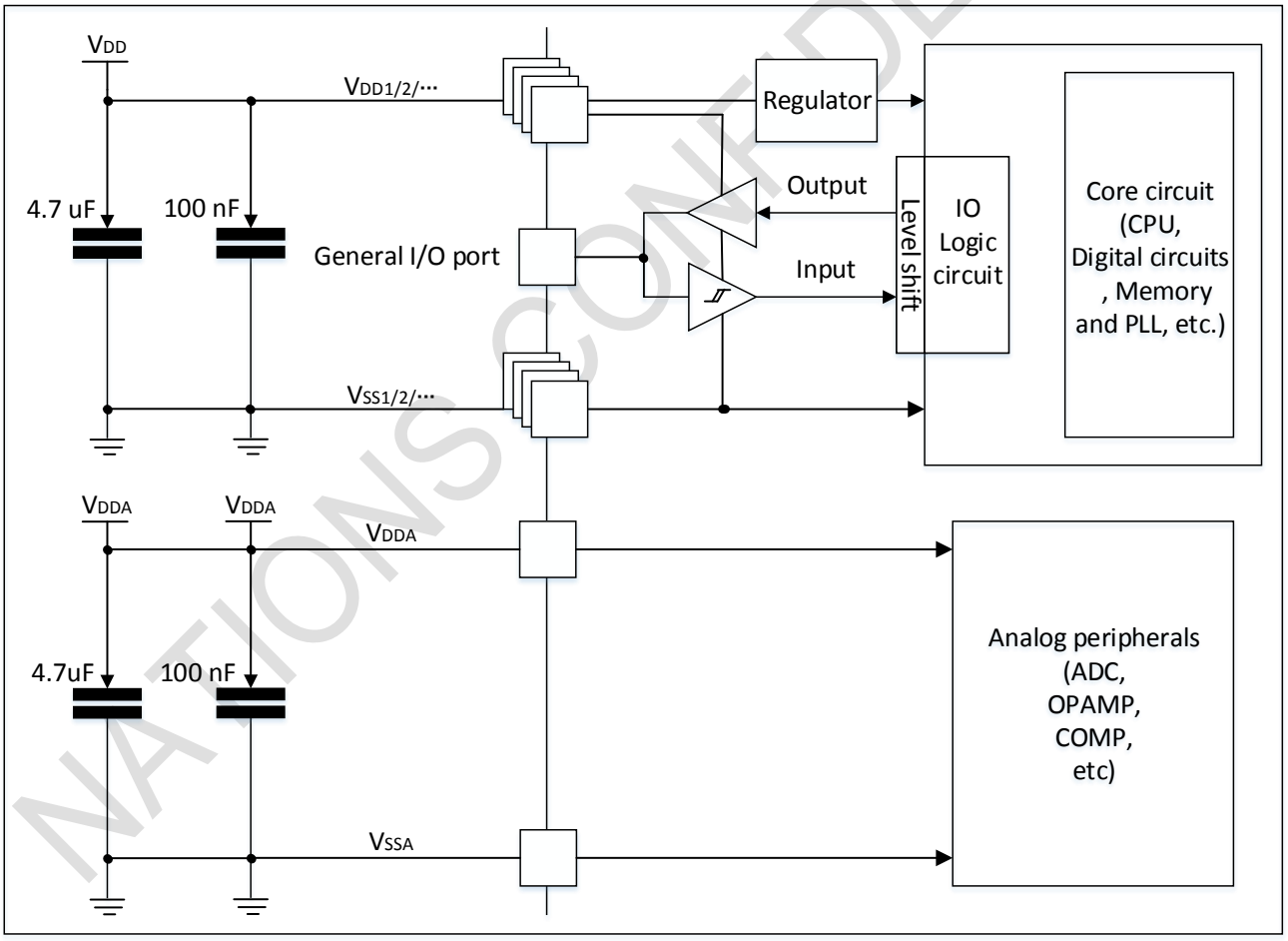
Figure 4-2 Pin input voltage



4.1.6 Power supply scheme

Figure 4-3 Power supply scheme



Note: V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS} respectively.

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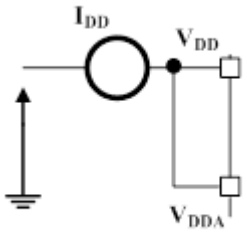
4.1.7 Current consumption measurement

Figure 4-4 Current consumption measurement



4.2 Absolute maximum ratings

The maximum ratings are the limits to which the device can be subjected without permanently damaging the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Table 4-1 Voltage characteristics

Symbol	Parameter	Min	Max	Unit
V_{DD}- V_{SS}	External supply voltage(including V_{DDA} and V_{DD})	-0.3	5.5	V
V_{IN}	Input voltage on 5V tolerant pins	V_{SS}-0.3	5.5	
	Input voltage on any other pins	V_{SS}-0.3	V_{DD} + 0.3	
$\lvert \Delta V_{DDx} \rvert$	Voltage difference between different power supply pins	-	50	mV
$\lvert V_{SSx}$- $V_{SS} \rvert$	Voltage difference between different ground pins	-	50	
$V_{ESD(HBM)}$	ESD electrostatic discharge voltage (human body model)	See section 4.4.10		

Table 4-2 Current characteristics

Symbol	Parameter	Max	Unit
I_{VDD}	Total current into V_{DD}/V_{DDA} power lines	200	mA
I_{VSS}	Total current out of V_{SS} ground lines	200	
I_{IO}	Maximum output current sunk for GPIO pins	16	
	Maximum output current sourced for GPIO pins	-16	
$I_{INJ(PIN)}$	Injection current of NRST pin	0/-5	
	Injection current of OSC_IN pin of HSE and OSC_IN pin of LSE	+/-5	
	Injection current of other pins	+/-5	
$\sum I_{INJ(PIN)}$(2)	Total injection current on all I/O and control pins	+/-16	

Table 4-3 Temperature characteristics

Symbol	Parameter	Value	Unit
T_{STG}	Storage temperature range	-40 ~ + 150	℃
T_J	Maximum junction temperature	125	℃

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4.3 Operating conditions

4.4 General operating conditions

Table 4-4 General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	AHBclock frequency	-	0	48	MHz
f_{PCLK1}	APB1clock frequency	-	0	48	
f_{PCLK2}	APB2clock frequency	-	0	48	
V_{DD}	Standard operating voltage	-	1.8	5.5	V
V_{DDA}	Analog operating voltage	Must be the same voltage as V_{DD}(1)	1.8	5.5	V
T_A	Temperature range	Maximum power consumption	-40	105	℃
T_J	Junction temperature range		-40	125	℃

1. Use the same power supply to supply V_{DD} and V_{DDA}. During power-up and normal operation, a maximum difference of 300mV between V_{DD} and V_{DDA} is allowed.
2. If T_A is lower, as long as T_J does not exceed $T_J$max, a higher PD value is allowed.
3. In the lower power dissipation state, as long as T_J does not exceed $T_J$max, T_A can be extended to this range.

4.4.1 Operating conditions at power-up and power-down

The parameters given in the following table are based on testing under the ambient temperature listed in Table 4-4.

Table 4-5 Operating conditions at power-up and power-down

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	From 0 to V_{DD}	100	∞	μs/V
	V_{DD} fail time rate	From V_{DD} to 0	100	∞	μs/V

4.4.2 Reset and power control module features

The parameter test conditions in the following table are based on Table 4-4.

Table 4-6 Reset and power control module features

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD}	Rising	PLS[3:0]=0	1.8	1.88	1.96	V
	Falling	PLS[3:0]=0	1.7	1.78	1.86	
	Rising	PLS[3:0]=1	2	2.08	2.16	
	Falling	PLS[3:0]=1	1.9	1.98	2.06	
	Rising	PLS[3:0]=2	2.2	2.28	2.36	
	Falling	PLS[3:0]=2	2.1	2.18	2.26	
	Rising	PLS[3:0]=3	2.4	2.48	2.56	
	Falling	PLS[3:0]=3	2.3	2.38	2.46	
	Rising	PLS[3:0]=4	2.6	2.68	2.76	
	Falling	PLS[3:0]=4	2.5	2.58	2.66	

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	Rising	PLS[3:0]=5	2.8	2.88	2.96	
	Falling	PLS[3:0]=5	2.7	2.78	2.86	
	Rising	PLS[3:0]=6	3	3.08	3.16	
	Falling	PLS[3:0]=6	2.9	2.98	3.06	
	Rising	PLS[3:0]=7	3.2	3.28	3.36	
	Falling	PLS[3:0]=7	3.1	3.18	3.26	
	Rising	PLS[3:0]=8	3.4	3.48	3.56	
	Falling	PLS[3:0]=8	3.3	3.38	3.46	
	Rising	PLS[3:0]=9	3.6	3.68	3.76	
	Falling	PLS[3:0]=9	3.5	3.58	3.66	
	Rising	PLS[3:0]=10	3.8	3.88	3.96	
	Falling	PLS[3:0]=10	3.7	3.78	3.86	
	Rising	PLS[3:0]=11	4	4.08	4.16	
	Falling	PLS[3:0]=11	3.9	3.98	4.06	
	Rising	PLS[3:0]=12	4.2	4.28	4.36	
	Falling	PLS[3:0]=12	4.1	4.18	4.26	
	Rising	PLS[3:0]=13	4.4	4.48	4.56	
	Falling	PLS[3:0]=13	4.3	4.38	4.46	
	Rising	PLS[3:0]=14	4.6	4.68	4.76	
	Falling	PLS[3:0]=14	4.5	4.58	4.66	
	Rising	PLS[3:0]=15	4.8	4.88	4.96	
	Falling	PLS[3:0]=15	4.7	4.78	4.86	
$V_{PVDhyst}$(2)	PVD hysteresis	-	80	100	125	mV
$V_{POR/PDR}$	VDD power on/power down reset threshold	-	-	1.53	-	V
$T_{RSTTEMPO}$(2)	Reset temporization	-	-	150		us

1. The characteristics of the product are guaranteed by design to the smallest value $V_{POR/PDR}$.
2. Guaranteed by design and comprehensive evaluation, not tested in production.

4.4.3 Internal reference voltage

The parameter test conditions in the following table are based on Table 4-4.

Table 4-7 Internal reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	-40℃< T_A< +105℃	1.16	1.21	1.26	V
$T_{S\_vrefint}$(1)	ADC sampling and read out the internal reference voltage time	PLS[2:0]=001 (Rising edge)	-	10	-	μs

1. The shortest sampling time is obtained through multiple cycles in the application.

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4.4.4 Current characteristics

The measurement method of current consumption is illustrated in Figure 4-4.

Maximum current consumption

The chip test conditions are as follows:

- All I/O pins are in input mode and connected to a static level-V_{DD} or V_{SS} (no load).
- All peripherals are in the off state, unless otherwise specified.
- The access time of flash memory is adjusted to the frequency of fHCLK (0~18MHz is 0 waiting period, 18~36MHz is 1 waiting period, and more than 36MHz is 2 waiting periods).
- The command prefetch function is enabled (Note: this parameter must be set before setting the clock and bus frequency division).
- When the peripheral is turned on: $f_{PCLK1} = f_{HCLK}$, $f_{PCLK2} = f_{HCLK}$.

The parameter test conditions in the following table are based on Table 4-4.

Table 4-8 Maximum current consumption in RUN mode when running code from FLASH

Symbol	Parameter	Conditions	f_{HCLK}	Typ (1) T_A = 105℃	Unit
I_{DD}	Supply current in RUN mode	External clock (2), Enable all peripherals	48MHz	8.4	mA
			24MHz	5.0	
			8MHz	2.8	
		External clock (2), Disable all peripherals	48MHz	5.0	
			24MHz	3.3	
			8MHz	2.3	

1. Guaranteed by design and comprehensive evaluation, not tested in production.
2. External clock, when f_{HCLK} is 24M or 48M, PLL needs to be enabled.

Table 4-9 Maximum current consumption in RUN mode when running code from RAM

Symbol	Parameter	Conditions	f_{HCLK}	Typ (1) T_A = 105℃	Unit
I_{DD}	Supply current in RUN mode	External clock (2), Enable all peripherals	48MHz	6.2	mA
			24MHz	4.1	
			8MHz	3.2	
		External clock (2), Disable all peripherals	48MHz	4.4	
			24MHz	3.2	
			8MHz	2.6	

1. Guaranteed by design and comprehensive evaluation, not tested in production.
2. External clock, when f_{HCLK} is 24M or 48M, PLL needs to be enabled.

Table 4-10 Maximum current consumption in SLEEP mode when running code from Flash

Symbol	Parameter	Conditions	f_{HCLK}	Typ (1) T_A = 105℃	Unit
I_{DD}	Supply current in SLEEP mode	External clock (2), Enable all peripherals	48MHz	6.5	mA
			24MHz	3.9	
			8MHz	2.0	

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		External clock (2), Disable all peripherals	48MHz	2.9	
			24MHz	2.1	
			8MHz	1.4	

1. Guaranteed by design and comprehensive evaluation, not tested in production.
2. External clock, when f_{HCLK} is 24M or 48M, PLL needs to be enabled.

Table 4-11 Typical consumption in PD mode and STOP mode

Symbol	Parameter	Conditions	Typ (1)	Max	Unit
			V_{DD}=3.3V	V_{DD}=3.3V	
Low power mode	Current in SLEEP mode	The core is stopped, all peripherals including Cortex®-M0 core peripherals, such as NVIC, system tick clock (SysTick) is still running)	2.7	5	mA
	Current in STOP mode	Turn off RTC, SRAM data retention, all I/O status retention, register retention	1.5	8	uA
	Current in PD mode	V_{DD} power-down mode, 3 WAKEUP IO and NRST can wake up the chip	0.5	1	uA

1. The typical value/maximum value is tested under T_A=25℃.

Typical current consumption

The chip test conditions are as follows:

- All I/O pins are in input mode and connected to a static level-V_{DD} or V_{SS} (no load).
- All peripherals are in the off state, unless otherwise specified.
- The access time of flash memory is adjusted to the frequency of fHCLK (0~18MHz is 0 waiting period, 18~36MHz is 1 waiting period, and more than 36MHz is 2 waiting periods).
- The command prefetch function is enabled (Note: this parameter must be set before setting the clock and bus frequency division).
- When the peripheral is turned on: f_{PCLK1}= f_{HCLK}, f_{PCLK2} = f_{HCLK}, f_{ADCCLK} = f_{PCLK2}/3.

Table 4-12 Maximum current consumption in RUN mode when running code from FLASH

Symbol	Parameter	Conditions	f_{HCLK}	Typ(1)		Unit
				Enable all peripherals(2)	Disable all peripherals	
I_{DD}	Current in RUN mode	External high-speed clock (HSE), use AHB prescaler to reduce the frequency	48MHz	8.2	4.8	mA
			24MHz	5.0	3.3	
			8MHz	2.7	2.1	
		Internal high-speed RC oscillator (2) (HSI), using AHB prescaler to reduce the frequency	48MHz	7.6	4.3	mA
			24MHz	4.3	2.7	
			8MHz	2.1	1.5	

1. The typical value is obtained by testing at T_A=25℃ V_{DD}=3.3V.
2. The internal high-speed clock is 8MHz, and PLL is enabled when f_{HCLK} > 8MHz.

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Table 4-13 Maximum current consumption in SLEEP mode when running code from Flash or RAM

Symbol	Parameter	Conditions	f_{HCLK}	Typ(1)		Unit
				Enable all peripherals(2)	Disable all peripherals	
I_{DD}	Current in SLEEP mode	External high-speed clock (HSE), use AHB prescaler to reduce the frequency	48MHz	6.3	2.7	mA
			24MHz	3.7	2.0	
			8MHz	1.8	1.2	
		Internal high-speed RC oscillator (2) (HSI), using AHB prescaler to reduce the frequency	48MHz	5.7	2.1	mA
			24MHz	3.1	1.4	
			8MHz	1.2	0.6	

1. The typical value is obtained by testing at T_A=25℃ V_{DD}=3.3V.
2. The internal high-speed clock is 8MHz, and PLL is enabled when f_{HCLK} > 8MHz.

4.4.5 External clock source characteristics

High-speed external clock generated by external oscillator

The characteristic parameters in the following table are measured using a high-speed external clock source.

The parameter test conditions in the following table are based on Table 4-4.

Table 4-14 High-speed external clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	External high-speed clock frequency	-	4	8	20	MHz
V_{HSEH}	OSC_IN input pin high level voltage (1)		0.7V_{DD}	-	V_{DD}	V
V_{HSEL}	OSC_IN input pin low-level voltage (1)		V_{SS}	-	0.3V_{DD}	
$t_{w(HSE)}$ $t_{w(HSE)}$	OSC_IN high or low time (1)		16	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time (1)		-	-	20	
$C_{in(HSE)}$	OSC_IN input capacitive reactance (1)		-	5	-	pF
$DuCy_{(HSE)}$	Duty cycle		45	-	55	%
I_L	OSC_IN input leakage current (1)	V_{SS}≤V_{IN}≤V_{DD}	-	-	±1	μA

1. Guaranteed by design and comprehensive evaluation, not tested in production.

Low-speed external clock generated by external oscillator source

The characteristic parameters in the following table are measured using a low-speed external clock source.

The parameter test conditions in the following table are based on Table 4-4.

Table 4-15 Low-speed external clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	External low-speed clock frequency	-	0	32.768	1000	KHz
V_{LSEH}	OSC32_IN input pin high level voltage (1)		0.7V_{DD}	-	V_{DD}	V
V_{LSEL}	OSC32_IN input pin low-level voltage (1)		V_{SS}	-	0.3V_{DD}	
$t_{w(LSE)}$ $t_{w(LSE)}$	OSC32_IN high or low time (1)		450	-	-	ns
$t_{r(LSE)}t_{f(LSE)}$	OSC32_IN rise or fall time (1)		-	-	10	
$DuCy_{(LSE)}$	Duty cycle (1)		30	-	70	%

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I_L	OSC32_IN input leakage current (1)	$V_{SS} \le V_{IN} \le V_{DD}$	-	-	±1	μA

1. Guaranteed by design and comprehensive evaluation, not tested in production.

Figure 4-5 AC timing diagram of external high-speed clock source

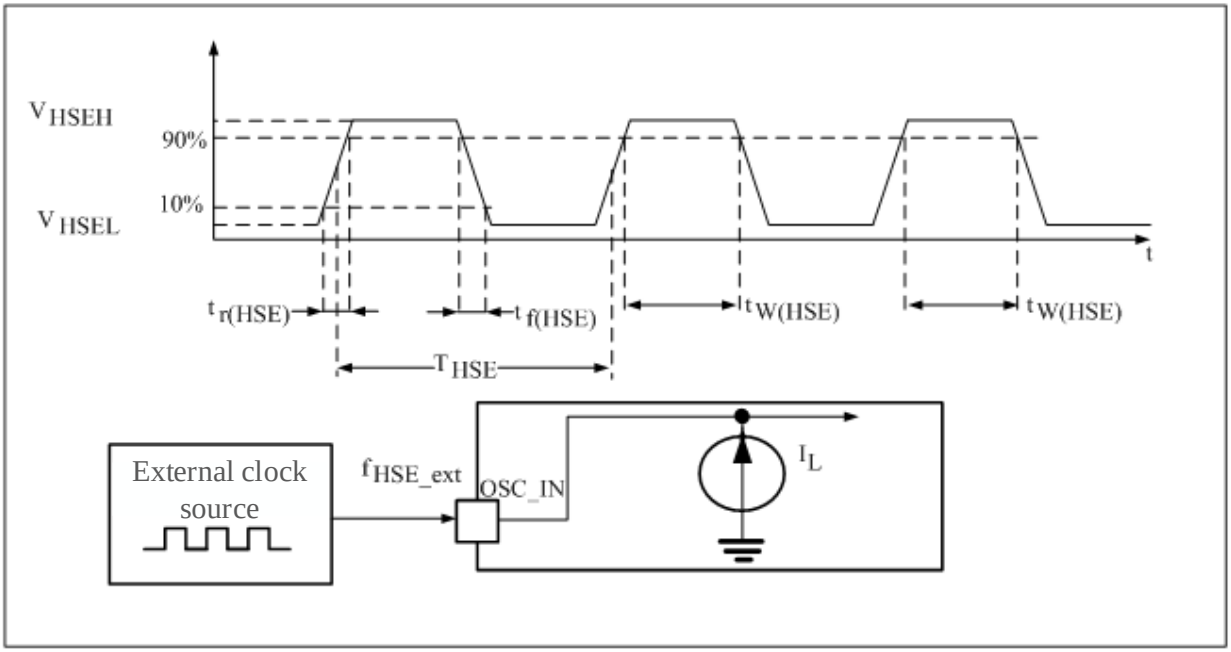
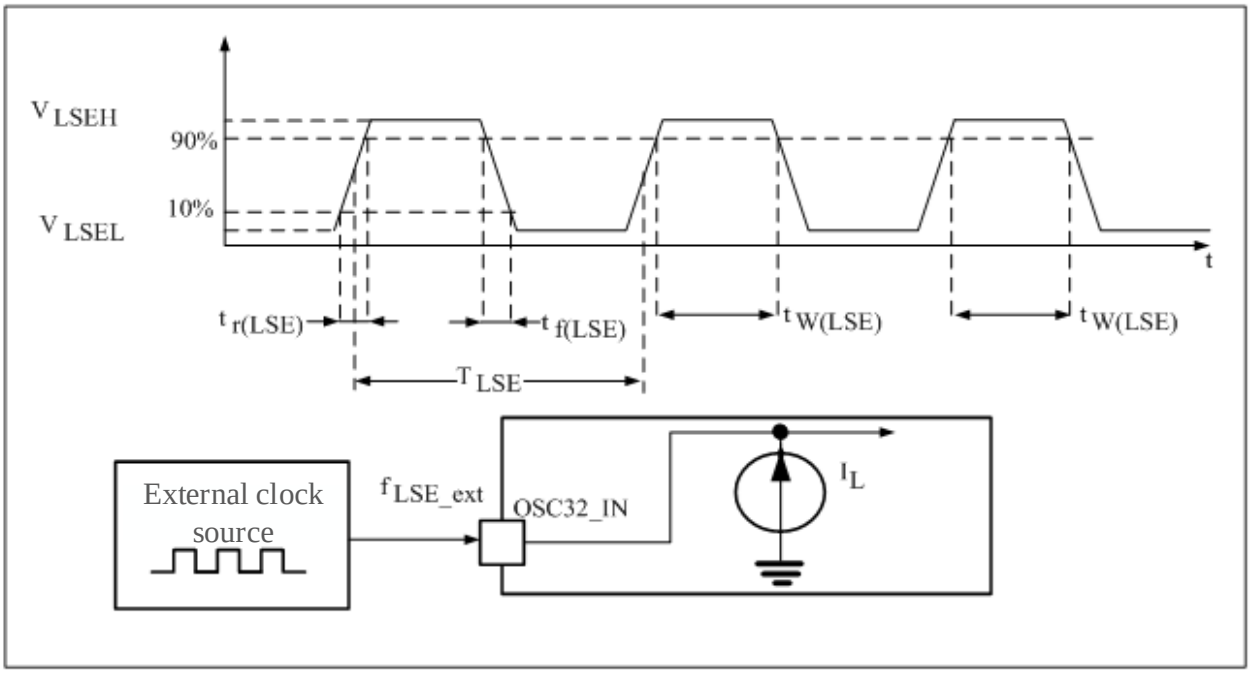


Figure 4-6 AC timing diagram of external low-speed clock source



High-speed external clock generated by a crystal/ceramic resonator

The high-speed external clock (HSE) can be generated using a 4-20MHz crystal/ceramic resonator oscillator. For detailed parameters (frequency, packaging, accuracy, etc.) of the crystal resonator, please consult the corresponding manufacturer. (The crystal resonator mentioned here is what we usually call passive crystal oscillator).

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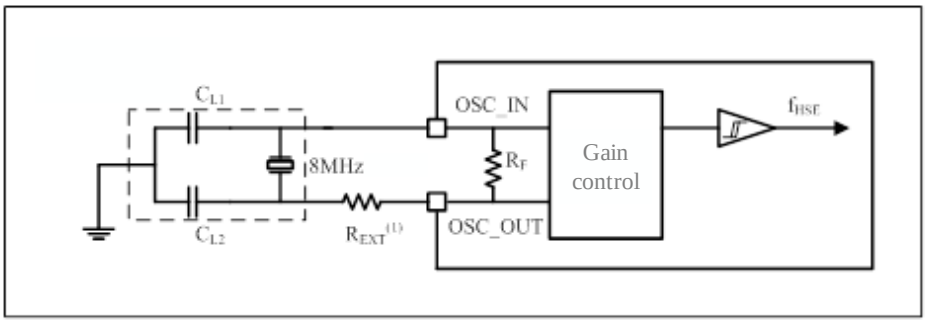
Table 4-16 HSE 4~20MHz Oscillator characteristics (1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency	-	4	8	20	MHz
C_{L1} C_{L2}(3)	Recommended load capacitance and corresponding crystal serial impedance (R_S)	R_S = 30Ω	-	20	-	pF
i_2	HSE driving current	V_{DD}=3.3V, V_{IN}=V_{SS} 30pF load	-	1.1	1.6	mA
$t_{SU(HSE)}$(4)	Startup Time	V_{DD} is stabilized	-	3	-	ms

1. The characteristic parameters of the resonator are given by the crystal/ceramic resonator manufacturer.
2. Guaranteed by design and comprehensive evaluation, not tested in production.
3. For C_{L1} and C_{L2}, it is recommended to use high-quality ceramic capacitors designed for high-frequency applications (typical value) between 5pF and 25pF, and select a crystal or resonator that meets the requirements. Usually C_{L1} and C_{L2} have the same parameters. The crystal manufacturer usually gives the parameter of the load capacitance in the serial combination of C_{L1} and C_{L2}. When choosing C_{L1} and C_{L2}, the capacitive reactance of PCB and MCU pins should be taken into consideration.
4. $t_{SU(HSE)}$ is the start-up time, which is the time from the software enabling HSE to start measurement until a stable 8MHz oscillation is obtained. This value is measured on a standard crystal resonator, and it may vary greatly depending on the crystal manufacturer.

Figure 4-7 Typical application using 8MHz crystal



1. R_{EXT} value is determined by the characteristics of the crystal.

Low-speed external clock generated by a crystal/ceramic resonator

The Low-speed external clock (LSE) can be generated using a 32.768 kHz crystal/ceramic resonator oscillator. For detailed parameters (frequency, packaging, accuracy, etc.) of the crystal resonator, please consult the corresponding manufacturer. (The crystal resonator mentioned here is what we usually call passive crystal oscillator).

Note: For C_{L1} and C_{L2}, it is recommended to use high-quality ceramic capacitors between 5pF and 15pF, and select a crystal or resonator that meets the requirements. Usually C_{L1} and C_{L2} have the same parameters. The crystal manufacturer usually gives the parameter of the load capacitance in the serial combination of C_{L1} and C_{L2}.

The load capacitance C_L is calculated by the following formula: $C_L = C_{L1} \times C_{L2} / (C_{L1} + C_{L2}) + Cstray$, where Cstray is the capacitance of the pin and the capacitance of the PCB board or PCB.

Table 4-17 LSE Oscillator characteristics (f_{LSE}=32.768 kHz) (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{L1} C_{L2}(2)	Recommended load capacitance and corresponding crystal serial impedance (R_S) (3)	R_S :30KΩ~65KΩ	-	-	20	pF
I2	LSE driving current	VDD=3.3V , CL1=CL2=12.5pF, R_S = 30KΩ	-	0.3	-	μA

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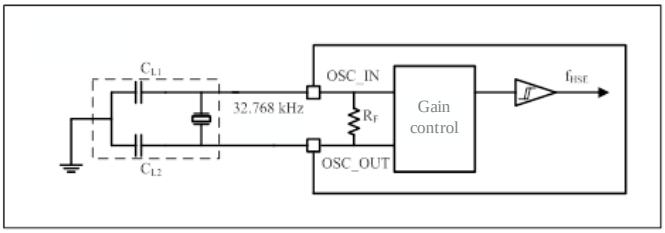
$t_{SU(LSE)}$(4)	Startup Time	V_{DD} is stabilized	-	2	-	s

1. Guaranteed by design and comprehensive evaluation, not tested in production.
2. See the caution paragraph at the top of this table.
3. Choose a high-quality oscillator with a smaller R_S value to optimize current consumption. Please consult the crystal manufacturer for details.
4. $t_{SU(LSE)}$ is the start-up time, which is the time from the software enabling LSE to start measurement until a stable 32.768KHz oscillation is obtained. This value is measured on a standard crystal resonator, and it may vary greatly depending on the crystal manufacturer.

Figure 4-8 Typical application using 32.768kH crystal



4.4.6 Internal clock source characteristics

The parameter test conditions in the following table are based on Table 4-4.

High-speed internal (HSI) RC oscillator

Table 4-18 HSI Oscillator characteristics (1) (2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency	V_{DD}=3.3V, T_A = 25℃, After calibration	7.92	8	8.08	MHz
ACC_{HSI}	The temperature drift of the HSI oscillator	V_{DD}=3.3V, T_A = -40~105℃, Temperature drift	-3	-	3	%
		V_{DD}=3.3V, T_A = -10~85℃, Temperature drift	-2.5	-	2	%
		V_{DD}=3.3V, T_A = 0~70℃, Temperature drift	-2	-	1.5	%
$t_{SU(HSI)}$	HSI Startup Time		1	-	3	μs
$I_{DD(HSI)}$	HSI driving current		-	80	150	μA

1. Unless otherwise specified, V_{DD} = 3.3V, T_A = -40~105℃.
2. Guaranteed by design and comprehensive evaluation, not tested in production.

Low-speed internal (HSI) RC oscillator

Table 4-19 LSI Oscillator characteristics (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
fLSI(2)	Frequency	V_{DD}=3.3V, T_A = 25℃, After calibration	29	30	31	KHz
		V_{DD} =1.8V ~5.5V, T_A = -40~105℃	24	30	36	KHz
$t_{SU(LSI)}$ (3)	LSI Startup Time		-	30	80	μs
$I_{DD(LSI)}$ (3)	LSI driving current		-	0.2	-	μA

1. Unless otherwise specified, V_{DD} = 3.3V, T_A = -40~105℃.
2. Guaranteed by design and comprehensive evaluation, not tested in production.

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4.4.7 Low-power mode wake-up time

The wake-up time listed in Table 4-20 is measured during the wake-up phase of an 8MHz HSI RC oscillator. The clock source used when waking up depends on the current operating mode:

- STOP or PD mode: clock source is RC oscillator
- SLEEP mode: the clock source is the clock used when entering sleep mode

The parameter test conditions in the following table are based on Table 4-4.

Table 4-20 Low-power mode wake-up time

Symbol	Parameter	Typ	Unit
$t_{WUSLEEP}$ (1)	Wake up from SLEEP mode	16	HCLK(2)
t_{WUSTOP} (1)	Wake up from STOP mode	20	us
t_{WUPD} (1)	Wake up from PD mode	55	

1. The measurement of the wake-up time is from the start of the wake-up event to the user program reading the first instruction.
2. HCLK is the AHB frequency.

4.4.8 PLL characteristics

The parameter test conditions in the following table are based on Table 4-4.

Table 4-21 PLL characteristics

Symbol	Parameter	Num			Unit
		Min	Typ	Max(1)	
f_{PLL_IN}	PLL input clock(2)	4	8.0	20	MHz
	PLL input clock duty cycle	40	-	60	%
f_{PLL_OUT}	PLL multiplier output clock	48	-	72	MHz
t_{LOCK}	PLL Ready indicates signal output time	-	-	50	μs
Jitter	TIE RMS Jitter	-	40	-	pS
Ipll	Operating Current of PLL @48MHz VCO frequency.	-	300	500	uA

1. Guaranteed by design and comprehensive evaluation, not tested in production.
2. Need to pay attention to using the correct frequency multiplication factor, so that f_{PLL_OUT} is within the allowable range according to the PLL input clock frequency.

4.4.9 FLASH characteristics

Unless otherwise specified, all characteristic parameters are obtained at T_A = -40~105℃.

Table 4-22 FLASH characteristics

Symbol	Parameter	Conditions	Min(1)	Typ(1)	Max(1)	Unit
tprog	Word programming time(32-bit)	T_A = -40~105℃	-	175	-	μs
t_{ERASE}	Page erase time(512Bytes)	T_A = -40~105℃	-	2.27	-	ms
t_{ME}	Mass erase time	T_A = -40~105℃;	-	34.1	-	ms

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I_{DD}	Current(1)	Read, f_{HCLK}=48MHz, V_{DD}=3.3V	-	2	2.4	mA
		Write, f_{HCLK}=48MHz, V_{DD}=3.3V	-	-	1.2	mA
		Erase, f_{HCLK}=48MHz, V_{DD}=3.3V	-	-	0.6	mA
		PD mode, V_{DD}=3.3~3.6V	-	-	150	μA

1. Guaranteed by design and comprehensive evaluation, not tested in production.

Table 4-23 Flash memory life and data retention period

Symbol	Parameter	Conditions	Min(1)	Unit
N_{END}	Endurance(Note: erasing and writing cycle)	T_A = -40~105 ℃	100	kcycles
t_{RET}	Data retention	T_A = 105 ℃, after 1000 erasing and cycle	10	years

1. Guaranteed by design and comprehensive evaluation, not tested in production.

4.4.10 Electrical sensitivity

Based on three different tests (ESD, LU), a specific measurement method is used to conduct a strength test on the chip to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

This test complies with the JESD22-A114/C101 standard.

Table 4-24 ESD characteristics

Symbol	Parameter	Conditions	Class	Min(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 ℃, conforming to JESD22-A114	2	4000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charging device model)	T_A = +25 ℃, conforming to JESD22-C101	II	1000	

1. Guaranteed by design and comprehensive evaluation, not tested in production.

Staic Latch-up

This test complies with the EIA/JESD78A integrated circuit latch standard.

Table 4-25 Staic Latch-up characteristics

Symbol	Parameter	Conditions	Class
LU	Staic Latch-up	T_A = +105 ℃, conforming to JESD 78A	II level A

4.4.11 I/O port characteristics

Generic input/output characteristics

The parameter test conditions in the following table are based on Table 4-4. All I/O ports are CMOS and TTL compatible.

Table 4-26 I/O static characteristics

Symbol	Parameter	VDD	Conditions	Min	Max	Unit
VIL	Standard IO Low level input	5	-	-	0.3×VDD	V

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	voltage	3.3	-	-	0.8	
		1.8	-	-	0.2×VDD	
VIH	Standard IO High level input voltage	5	-	0.7×VDD	-	
		3.3	-	2.0	-	
		1.8	-	0.8×VDD	-	
Vhys	I/O Schmitt trigger voltage hysteresis (1)	5/3.3/1.8	-	0.1×VDD	---	V
Ilkg(2)	Input leakage current IIH	5/3.3/1.8	-	---	+1	µA
	Input leakage current IIL	5/3.3/1.8	-	-1	-	
VOH	Output high level voltage	5	High driving Imin=16mA low driving Imin=8mA	VDD-0.8	-	V
		3.3	High driving Imin=8mA low driving Imin=4mA	2.4	-	
		1.8	High driving Imin=4mA low driving Imin=2mA	VDD-0.45	-	
VOL	Output low level voltage	5	High driving Imin=16mA low driving Imin=8mA	-	0.7	
		3.3	High driving Imin=8mA low driving Imin=4mA	-	0.45	
		1.8	High driving Imin=4mA low driving Imin=2mA	-	0.4	
RPU	Internal pull-up resistor	5/3.3/1.8	-	40	100	kΩ
RPD	Internal pull-down resistor	5/3.3/1.8	-	40	100	kΩ
CIO	I/O pin capacitance	5/3.3/1.8	-	-	10	pF

1. The hysteresis voltage of the Schmitt trigger switching level. Guaranteed by design and comprehensive evaluation, not tested in production.
2. If there is reverse current in the adjacent pin, the leakage current may be higher than the maximum value.

Input and output AC characteristics

The parameter test conditions in the following table are based on Table 4-4.

Table 4-27 I/O AC characteristics

VDD	Conditions			Rise/Fall Time (ns)			Propagation Delay (ns)		
	Driving Strength	Slew Rate Control	CLoading(pf)	Min	Typ	Max	Min	Typ	Max
5V (4.5~5.5)	Low (DR=1)	Slow (SR=1)	25	3.1	3.9	6.5	5	7.2	14
			50	5.7	6.5	11	6.5	8.8	16
			100	11	13	20	10	12	21

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VDD	Conditions			Rise/Fall Time (ns)			Propagation Delay (ns)		
	Driving Strength	Slew Rate Control	CLoading(pf)	Min	Typ	Max	Min	Typ	Max
3.3V (2.7~3.6)	High (DR=0)	Fast (SR=0)	25	2.9	3.4	5.4	4.5	6.5	12
			50	5.6	6.3	10	6	8.1	14.2
			100	11	12.3	19.5	9	11.3	19.1
		Slow (SR=1)	25	1.8	2.5	4.1	4.2	6.7	13
			50	3	3.9	6.2	5	7.5	15
			100	5.6	6.5	10.2	6.4	9	17
	Low (DR=1)	Fast (SR=0)	25	1.6	2.1	3.4	3.7	5.9	12
			50	2.9	3.5	5.5	4.4	6.6	13
			100	5.5	6.2	10	5.9	8	15
		Slow (SR=1)	25	4	5.5	11	6.6	10	20
			50	7.5	9.5	18	8.5	12	24
			100	15	17	32	13	16	31
		Fast (SR=0)	25	3.8	4.9	9.2	5.9	8.8	18
			50	7.3	8.8	16.2	7.8	10.8	21.2
			100	14.2	16.7	30.5	12	15	29
	High (DR=0)	Slow (SR=1)	25	2.4	3.7	7.2	5.5	8.5	17.1
			50	3.9	5.5	10.5	6.5	9.6	19.2
			100	7.3	9.3	17.2	8.4	12	23
		Fast (SR=0)	25	2	3.1	5.9	4.9	7.6	16
			50	3.7	4.9	9.5	5.8	8.7	18
			100	7.2	8.8	17	7.7	11	22
1.8V (1.62~1.98)	Low (DR=1)	Slow (SR=1)	25	8	12	22	14	23	44
			50	15	20	36	18	27	52
			100	29	36	65	26	36	66
		Fast (SR=0)	25	7.5	10.5	16.4	12.25	20	40
			50	14.5	18.5	33	16.5	24.2	47
			100	28	35	62	24	33	62
	High (DR=0)	Slow (SR=1)	25	4.6	8	15.4	12	20.2	40
			50	7.6	11.8	22	14	22.5	44
			100	11.5	19.5	36	17.5	26.7	52
		Fast (SR=0)	25	4	6.9	14	10.5	18	36
			50	7.3	11	20	12.3	20	40

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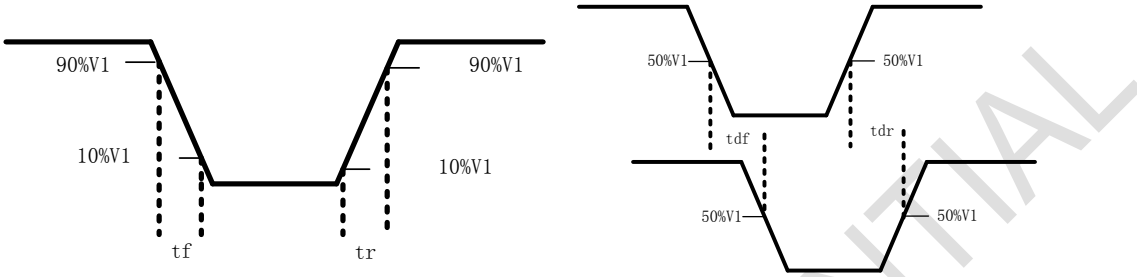
VDD	Conditions			Rise/Fall Time (ns)			Propagation Delay (ns)		
	Driving Strength	Slew Rate Control	CLoading(pf)	Min	Typ	Max	Min	Typ	Max
			100	15	18.5	33	16	25	47

Figure 4-9 I/O AC characteristic definition



4.4.12 NRST pin characteristics

NRST pin input driver uses CMOS technology. NRST pin is connected to a pull-up resistor that cannot be disconnected.

The parameter test conditions in the following table are based on Table 4-4.

Table 4-28 NRST pin characteristics

Symbol	Parameter	VDD	Min	Typ	Max	Unit
$V_{IL(NRST)}$(1)	NRST low level input voltage	1.8V~5.5V	-	-	0.3VDD	V
$V_{IH(NRST)}$(1)	NRST high level input voltage	1.8V~5.5V	0.5VDD	-	-	
$V_{hys(NRST)}$	NRST schmitt trigger voltage hysteresis	1.8V~5.5V	115	220	315	mV
VOL	nrst output low voltage	1.8v~2.7v, Iol=1.5mA	-	-	0.1	V
		1.8v~2.7v, Iol=2mA	-	-		
		1.8v~2.7v, Iol=3mA	-	-		
R_{PU}	Internal pull-up resistor (2)	1.8V~5.5V	30	40	50	kΩ
$V_{F(NRST)}$(1)	NRST input filter pulse	1.8V~2V	-	-	100	ns
		3V~3.6V	-	-	100	
		4.5V~5.5V	-	-	50	
$V_{NF(NRST)}$(1)	NRST input unfiltered pulse	1.8V~2V	650	-	-	ns
		3V~3.6V	300	-	-	
		4.5V~5.5V	200	-	-	

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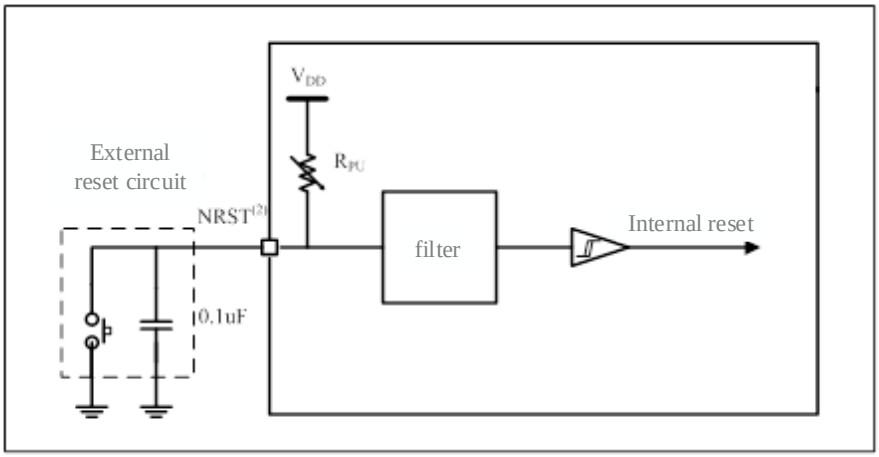
Figure 4-10 NRST pin protection recommended circuit design



1. The reset network is to prevent parasitic reset.
2. The user must ensure that the potential of the NRST pin can be lower than the maximum $V_{IL\ (NRST)}$, otherwise the MCU cannot be reset.

4.4.13TIM characteristics

Table 4-29 TIM (1) characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	$f_{TIMxCLK}$= 48MHz	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$= 48MHz	20.8	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH2	$f_{TIMxCLK}$= 48MHz	0	$f_{TIMxCLK}$/2	MHz
		$f_{TIMxCLK}$= 48MHz	0	24	MHz
Res_{TIM}	Timer resolution	$f_{TIMxCLK}$= 48MHz	-	16	bit
$t_{COUNTER}$	Select the internal clock, 16-bit counter clock cycle	$f_{TIMxCLK}$= 48MHz	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$= 48MHz	0.0208	1365	µs
t_{MAX_COUNT}	Maximum count	$f_{TIMxCLK}$= 48MHz	-	65536x65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$= 48MHz	-	89.478	s

1. TIM1/TIM8.

4.4.14I2C characteristics

The parameter test conditions in the following table are based on Table 4-4.

The I2C interface complies with the standard I2C communication protocol.

But SDA and SCL are not "true" open-drain pins. When configured as open-drain output, the PMOS tube between the pin and VDD is turned off, but it still exists.

Table 4-30 I2C interface characteristics

Symbol	Parameter	Standard model		Fast mode		Fast+ mode		Unit
		Min	Max	Min	Max	Min	Max	
fSCL	I2C interface frequency	0	100	0	400	0	1000	KHz
th(STA)	Start condition holding time (1)	4.0	-	0.6	-	0.26	-	µs

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tw(SCLL)	SCL Clock Low Time (1)	4.7	-	1.3	-	0.5	-	μs
tw(SCLH)	SCL clock high time (1)	4.0	-	0.6	-	0.26	-	μs
tsu(STA)	Establishment time of repeated starting conditions (1)	4.7	-	0.6	0.6	0.26	-	μs
th(SDA)	SDA data retention time (1)	-	3.4	-	0.9	-	0.4	μs
tsu(SDA)	Establishment time of SDA (1)	250.0	-	100	-	50	-	ns
tr(SDA) tr(SCL)	SDA and SCL rise time (1)	-	1000	20+0.1 Cb	300	-	120	ns
tf(SDA) tf(SCL)	SDA and SCL drop time (1)	-	300	20+0.1 Cb	300	-	120	ns
tsu(STO)	Time to establish the stop condition (1)	4.0	-	0.6	-	0.26	-	μs
tw(STO:STA)	Time from stop condition to start condition (bus idle) (1)	4.7	-	1.3	-	0.5	-	μs
Cb	Capacity load per bus (1)	-	400	-	400	-	200	pf
tv(SDA)	Data validity time(1)	3.45	-	0.9	-	0.45	-	μs
tv (ACK)	Response validity time (1)	3.45	-	0.9	-	0.45	-	μs

1. Guaranteed by design and comprehensive evaluation, not tested in production.
2. To achieve the maximum frequency of standard mode I2C, FPCLK1 must be greater than 2MHz.To achieve the maximum frequency of fast mode I2C, FPCLK1 must be greater than 4MHz.

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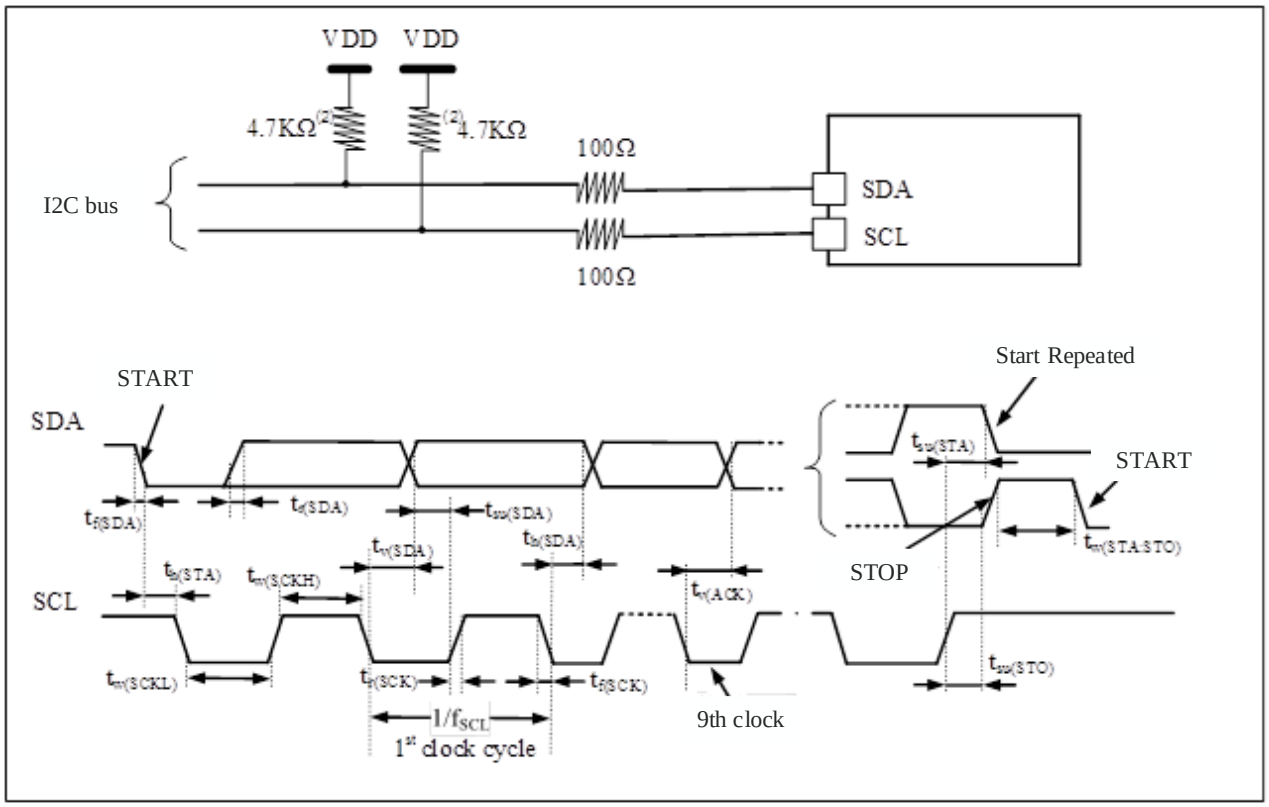
Figure 4-11 I2C bus AC waveform and measurement circuit (1)



1. The measuring point is set at the CMOS level: $0.3V_{DD}$ and $0.7V_{DD}$.

4.4.15 SPI/I2S characteristics

The parameter test conditions in the following table are based on Table 4-4.

Table 4-31 SPI characteristics (4)

Symbol	Parameter	Conditions		Min	Max	Unit
f_{SCLK} $1/t_{c(SCLK)}$	SPI clock frequency	Master mode		-	18	MHz
		Slave mode		-	18	
$t_{r(SCLK)}t_{f(SCLK)}$	SPI clock up and down time	Load capacitance: C = 30pF		-	8	ns
DuCy(SCK)	SPI from the input clock duty cycle	SPI Slave mode		30	70	%
$t_{su(NSS)}$ (1)	NSS establishment time	Slave mode		$4t_{PCLK}$	-	ns
$t_{h(NSS)}$(1)	NSS retention time	Slave mode		$2t_{PCLK}$	-	ns
$t_{w(SCLKH)}$(1) $t_{w(SCLKL)}$(1)	SCLK high and low time	Master mode		t_{PCLK}	t_{PCLK} + 2	ns
$t_{su(MI)}$(1)	Data entry setup time	Master mode	SPI1	19.84	-	ns
			SPI2	20.5	-	
$t_{su(SI)}$(1)		Slave mode	SPI1	4.16	-	
			SPI2	4.16	-	
$t_{h(MI)}$(1)	Data entry retention time	Master mode		0	-	ns
$t_{h(SI)}$(1)		Slave mode		4	-	

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$t_{a(SO)}$(1)(2)	Data output access time	Slave mode, fPCLK = 20MHz		0	$3t_{PCLK}$	ns
$t_{dis(SO)}$(1)(3)	Disabled time for data output	Slave mode		2	10	ns
$t_{v(SO)}$(1)	Valid time of data output	Slave mode (after the enabled edge)	Valid time of data output	-	32	ns
			SPI2	-	30	
$t_{v(MO)}$(1)		Mastermode (after the enabled edge)	SPI1	-	28	
			SPI2	-	28	
$t_{h(SO)}$(1)	Data output retention time	Slave mode (after the enabled edge)		0	-	ns
$t_{h(MO)}$(1)		Master mode (after the enabled edge)		0	-	

1. Guaranteed by design and comprehensive evaluation, not tested in production.
2. The minimum value means the minimum time to drive the output, and the maximum value means the maximum time to get the data correctly.
3. The minimum value means the minimum time to turn off the output, and the maximum value means the maximum time to put the data line in the high resistance state.
4. Test voltage is 3.3V.

Figure 4-12 SPI sequence diagram - slave mode and CPHA=0

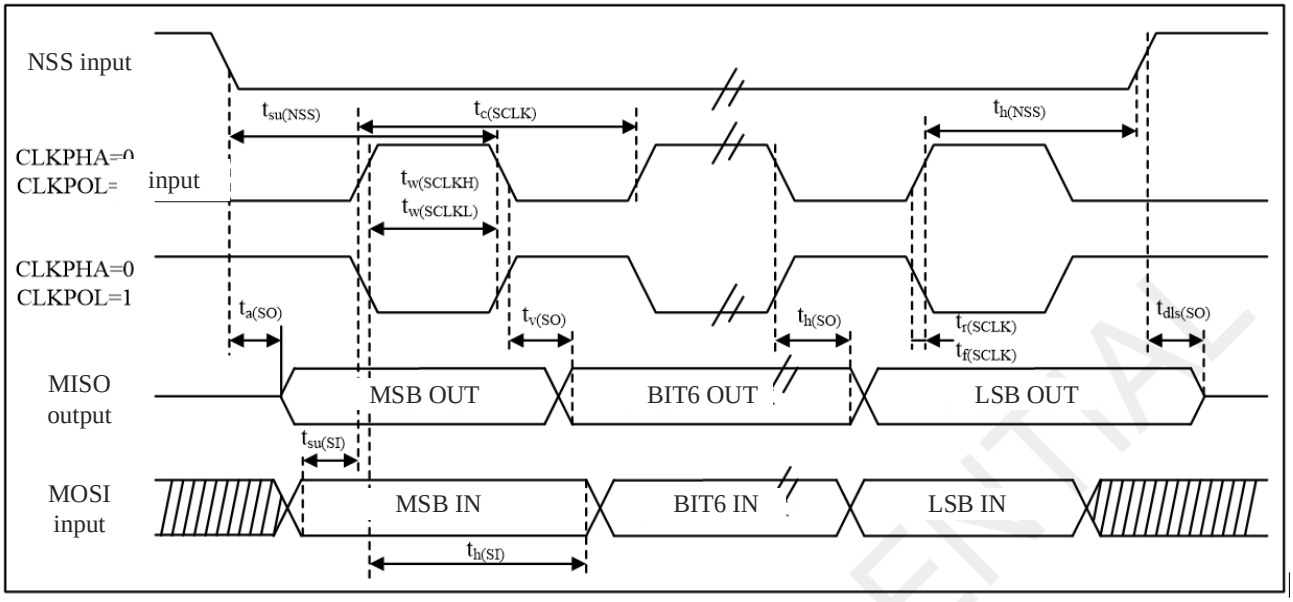

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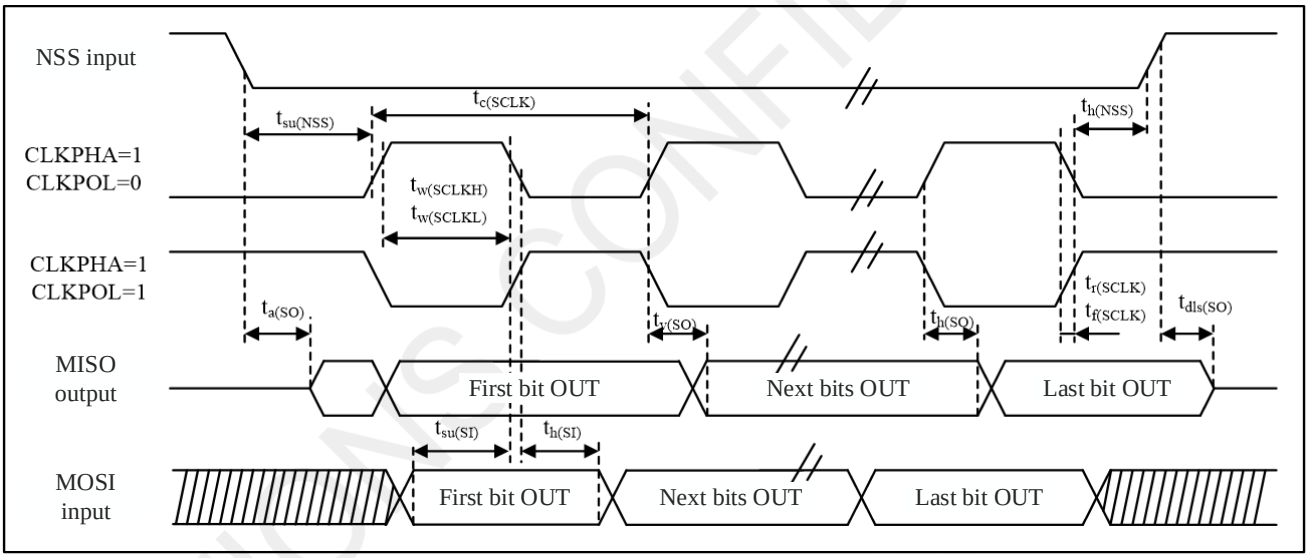
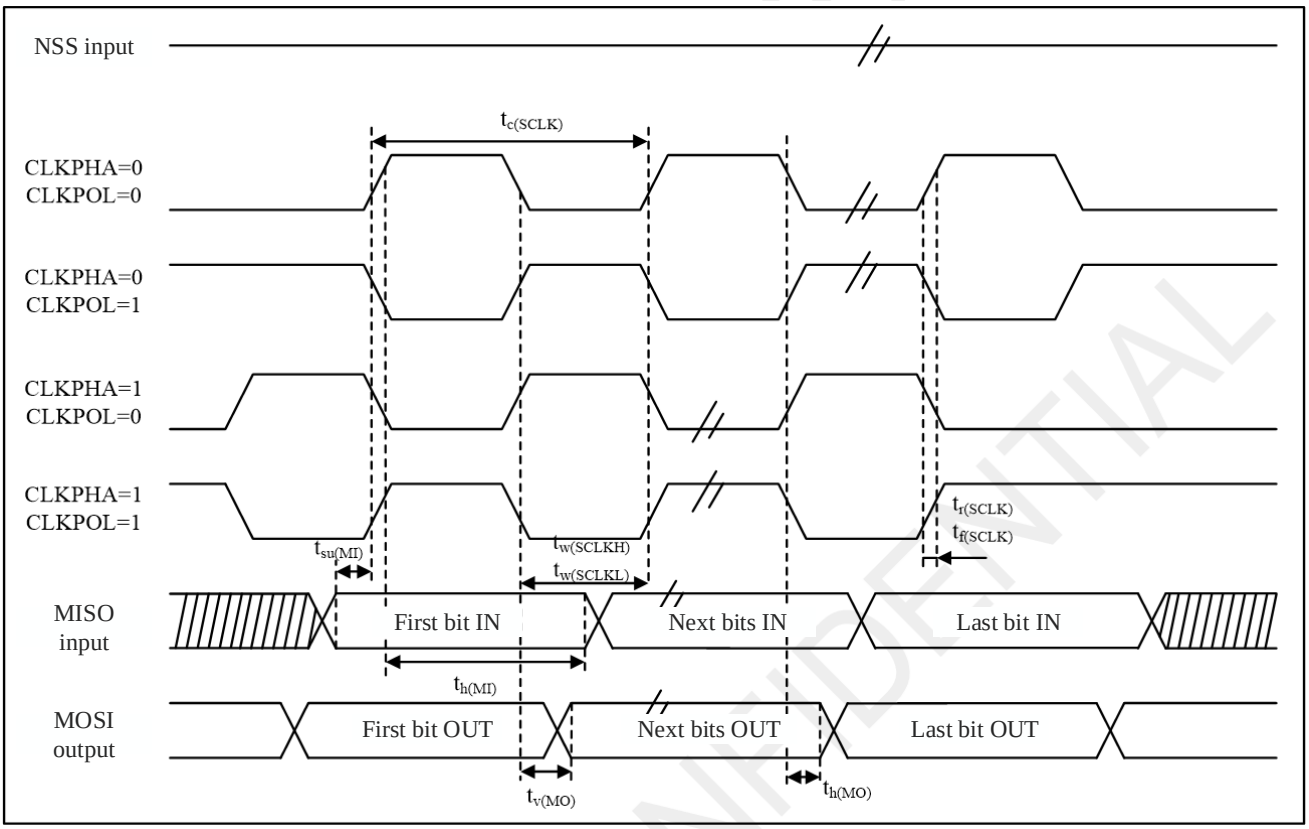
Figure 4-13 SPI sequence diagram - slave model and CPHA=1(1)



1. The measurement points were set at the CMOS level of 0.3 V_{DD} and 0.7 V_{DD}.

Figure 4-14 SPI timing diagram-master mode (1)



1. The measurement points are set at CMOS level: 0.3 V_{DD} and 0.7 V_{DD}.

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Table 4-32 I2S characteristics (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DuCy(SCK)	I2S from the input clock duty cycle	I2S Slave mode	30	50	70	%
f_{CLK} $1/t_{c(CLK)}$	I2S clock frequency	Master mode (16bit)	-	2*Fs(3)*16	-	Hz
		Master mode (16bit)	-	2*Fs(3)*16	-	
		Master mode (32bit)	-	2*Fs(3)*32	-	
		Slave mode (32bit)	-	2*Fs(3)*32	-	
$t_{r(CLK)}$	I2S clock up and down time	Load capacitance: CL = 50pF	-	-	8	ns
$t_{v(WS)}$ (1)	WS validity time	Master mode	13.5	-	-	
$t_{h(WS)}$(1)	WS retention time	Master mode	0	-	-	
$t_{su(WS)}$ (1)	WS establishment time	Slave mode	4	-	-	
$t_{h(WS)}$(1)	WS retention time	Slave mode	0	-	-	
$t_{w(CLKH)}$(1)	CLK high and low time	Master mode, fPCLK = 16MHz, audio 48kHz	312.5	-	-	
$t_{w(CLKL)}$(1)			345	-	-	
$t_{su(SD\_MR)}$(1)	Data entry setup time	master receiver	3.6	-	-	
$t_{su(SD\_SR)}$(1)		Slave receiver	3.5	-	-	
$t_{h(SD\_MR)}$(1)(2)	Data entry retention time	master receiver	0	-	-	
$t_{h(SD\_SR)}$(1)(2)		Slave receiver	0	-	-	
$t_{v(SD\_ST)}$(1)(2)	Valid time of data output	Slave transmitter (after the enabled edge)	-	-	29.76	ns
$t_{h(SD\_ST)}$(1)	Data output retention time	Slave generator(after the enabled edge)	0	-	-	
$t_{v(SD\_MT)}$(1)(2)	Valid time of data output	master generator(after the enabled edge)	-	-	13.6	
$t_{h(SD\_MT)}$(1)	Data output retention time	master generator(after the enabled edge)	-6.5	-	-	

1. Guaranteed by design and comprehensive evaluation, not tested in production.
2. Relying on f_{PCLK}.For example, if f_{PCLK}=8MHz, then T_{PCLK}=1/ f_{PCLK} =125ns.
3. FS value audio sampling frequency, frequency range 8 KHz ~ 96 KHz.

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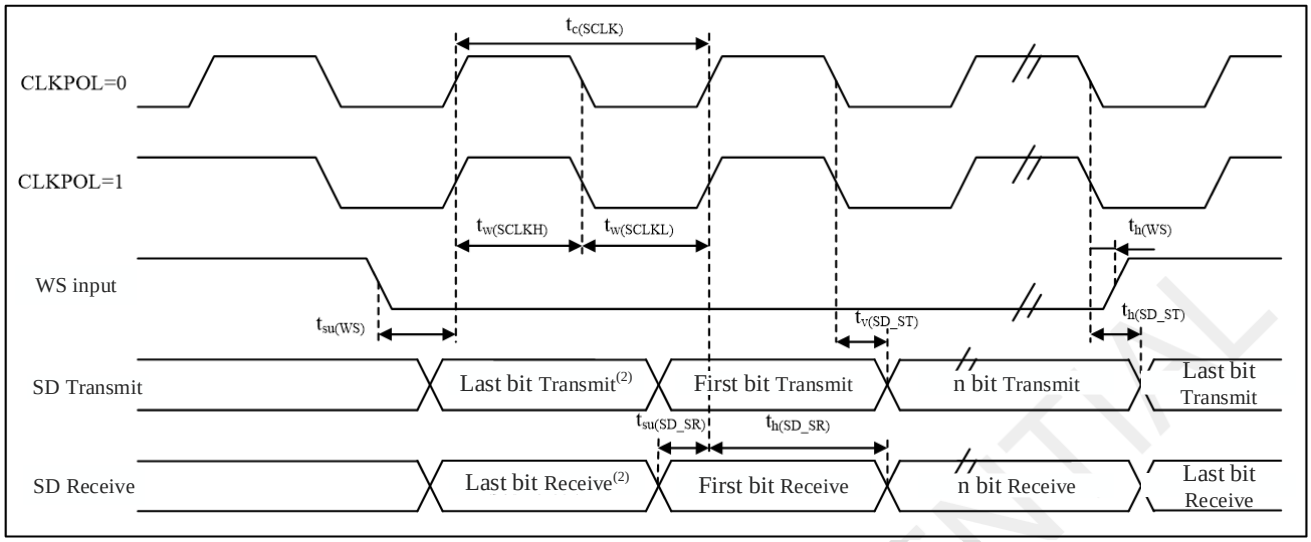
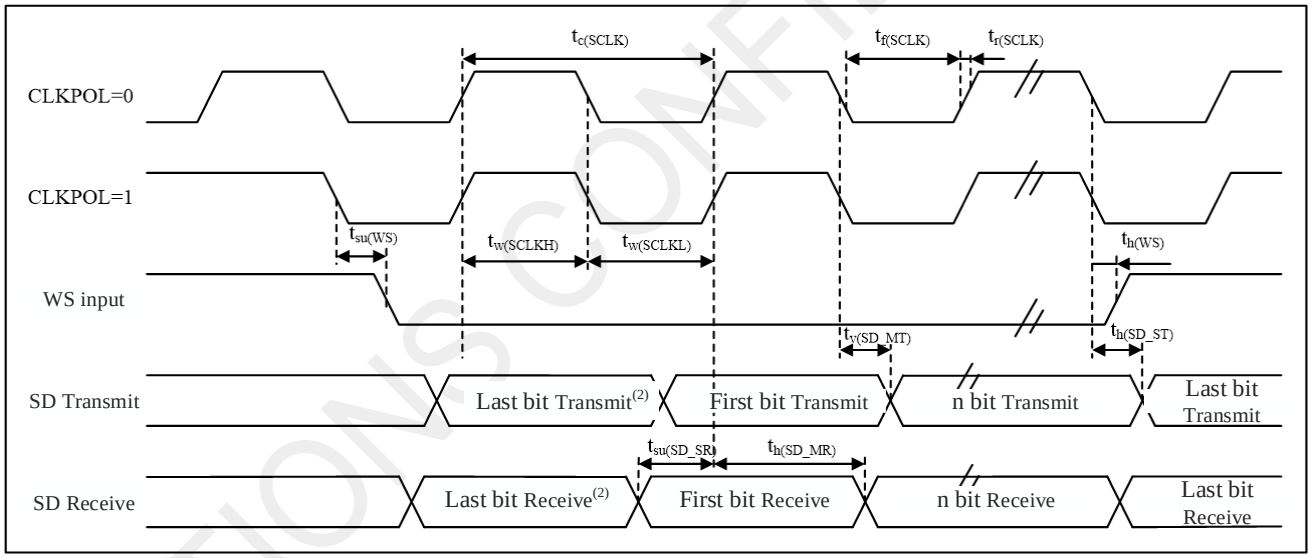
Figure 4-15 I2S slave mode timing diagram (Philips protocol) (1)



1. The measuring point is set at the CMOS level: 0. $3V_{DD}$ and 0. $7V_{DD}$.
2. Send/receive the lowest bit of the previous byte.There is no send/receive at the lowest level until the first byte.

Figure 4-16 I2S master mode timing diagram (Philips protocol) (1)



1. The measuring point is set at the CMOS level: 0. $3V_{DD}$ and 0. $7V_{DD}$.
2. Lowest send/receive of the previous byte. There is no send/receive before the first byte.

4.4.16 ADC characteristics

The parameter test conditions in the following table are based on Table 4-4.

Table 4-33 ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Supply voltage	-	2.4	3.3	5.5	V
V_{REF+}	Positive reference voltage	-	2.4	-	$V_{DD}A$	V
f_{ADC}	ADC clock frequency	-	-	-	18	MHz
f_s(1)	Sampling rate	-	-	0.89	1.33	Msps

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V_{AIN}	Conversion voltage range (2)	-	0	-	V_{REF+}	V
R_{AIN}(1)	External input impedance	-	See formula 1			Ω
R_{ADC}(1)	ADC input resistance	V_{DDA} =3.0v	-	1500	-	Ω
C_{ADC}(1)	Internal sample and hold capacitor	-	-	13	15	pF
SNDR	Singal noise distortion ration	V_{DDA} =3.3v	-	68	-	dB
t_S (1)	Sampling time	-	6	-	-	$1/f_{ADC}$
t_{STAB} (1)	Power-on time	-	32	-	-	$1/f_{ADC}$
t_{CONV} (1)	Conversion time	-	12			$1/f_{ADC}$

1. Guaranteed by design and comprehensive evaluation, not tested in production.
2. V_{REF+} is internally connected to V_{DDA}.

Formula 1: Maximum R_{AIN} formula

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

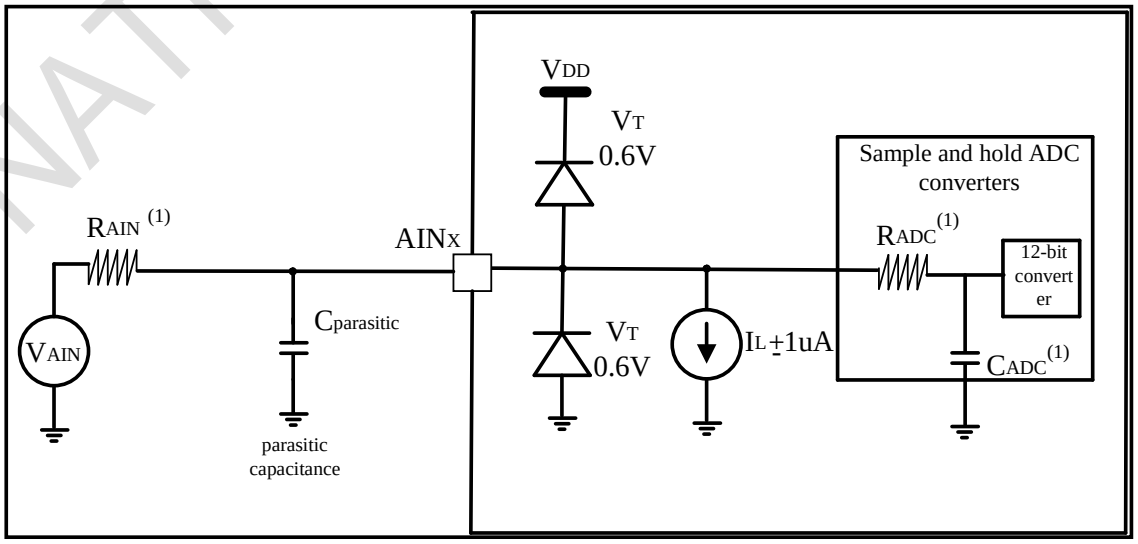
The above formula (Equation 1) is used to determine the maximum external impedance so that the error can be less than 1/4 LSB. Where N=12 (representing 12-bit resolution).

Table 4-34 ADC accuracy (1)(2)

Symbol	Parameter	Conditions	Typ	Max	Unit
EG	Gain error	V_{REF+} = 3.3V, T_A = 25 ℃, Vin = 0.05V_{DDA} ~ 0.95V_{DDA}	±2	±5	LSB
EO	Offset error		±0.5	±2.0	
ED	Differential linearity error		±0.6	1.5	
EL	Integral linearity error		±1.5	2.5	
ENOB	Effective number of bits		11	-	Bits

1. DC numerical accuracy of the ADC is measured after internal calibration.
2. ADC reverse relationship between the injection current and accuracy: the need to avoid reverse current is injected on any standard analog input pin, as this significantly reduces the ongoing analog input pin on the other of conversion accuracy. It is recommended to add a Schottky diode (between the pin and ground) on the standard analog pin that may produce reverse injection current.
3. Guaranteed by design and comprehensive evaluation, not tested in production.

Figure 4-17 ADC typical connection diagram



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4.4.17 OPAMP characteristics

The parameter test conditions in the following table are based on Table 4-4.

Table 4-35 OPAMP characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VDDA	Analog supply voltage	-	2.4	-	5.5	V
CMIR	Common mode voltage input range	-	0	-	VDDA	V
VIOFFSET	Input offset voltage	-	-	4	7	mV
ILOAD	Drive current	-	-	0.5	-	mA
IDDA	OPAMP current consumption	No load, quiescent mode	-	0.5	-	mA
CMMR	Common mode rejection ratio	-	-	70	-	dB
PSRR	Power supply rejection ratio	-	-	60	-	dB
GBW	Gain bandwidth	-	-	2.5	-	MHz
SR	Conversion rate	-		3	-	V/us
RLOAD	Minimum impedance load	-	10	-	-	KΩ
CLOAD	Maximum capacitive load	-	-	-	25	pF
TSTARTUP	Startup time	CLOAD ≤ 25 pf, RLOAD ≥ 10 kΩ, Follower configuration	-	3	5	μs
PGA BW	PGA bandwidth for different non inverting gain	PGA Gain = 2, Cload = 25pF, Rload = 10 KΩ	-	1	-	MHz
		GA Gain = 4, Cload = 25pF, Rload = 10 KΩ	-	0.5	-	
		GA Gain = 16, Cload = 25pF, Rload = 10 KΩ	-	0.125	-	
		GA Gain = 32, Cload = 25pF, Rload = 10 KΩ	-	0.0625	-	

1. Guaranteed by design and comprehensive evaluation, not tested in production.

4.4.18 COMP characteristics

The parameter test conditions in the following table are based on Table 4-4.

Table 4-36 COMP characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VDDA	Analog supply voltage	-	2.2	-	5.5	V
VIN	Input voltage range	-	0	-	VDDA	
TSTART	Comparator startup time	normal mode	-	-	5	us
		low speed mode			15	
td	Propagation delay for 200 mV step with 100 mV overdrive	VDDA>=2.2Vnormal mode	-	100		ns
		low speed mode		520		

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VOFFSET	Comparator input offset error	Full common mode range		-	±4	±20	mV
Vhys	Comparison of hysteresis voltage (high speed/low power consumption)	No hysteresis		-	0	-	mV
		Low hysteresis		-	10/8	-	
		Medium hysteresis		-	20/15	-	
		High hysteresis		-	30/25	-	
IDDA	Comparator current consumption	High speed mode	Static	-	35	-	µA
			With 50 kHz ±100 mV overdrive square signal	-	36	-	
		Low speed mode	Static	-	5	-	
			With 50 kHz ±100 mV overdrive square signal	-	6	-	

1. Guaranteed by design and comprehensive evaluation, not tested in production.

4.4.19 Temperature sensor characteristics

The parameter test conditions in the following table are based on Table 4-4.

Table 4-37 Temperature sensor characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	Linearity of V_{SENSE} with respect to temperature	-	±2	±4.5	℃
Avg_Slope(1)	Average slope	-	3.9	-	mV/℃
V_{25}(1)	Voltage at 25℃	-	1.3	-	V
t_{START}(1)	Startup time	-	11	22	µs
T_{S_temp}(1)(2)	ADC sampling time when reading the temperature	-	1.87	6.43	µs

1. Guaranteed by design and comprehensive evaluation, not tested in production.

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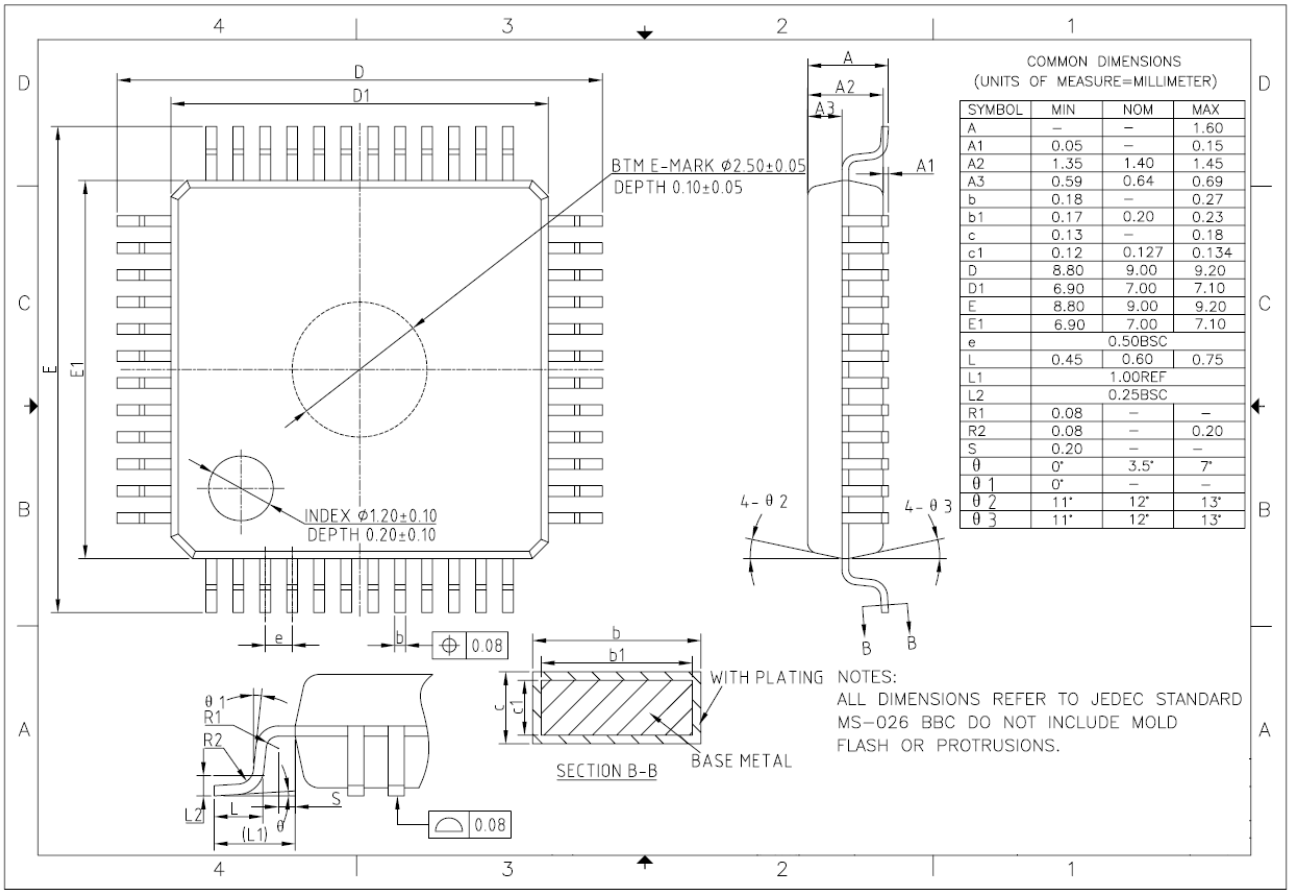
5 Package information

5.1 LQFP48

Figure 5-1 LQFP48 package outline



SYMBOL	MIN	NOM	MAX
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	–	0.27
b1	0.17	0.20	0.23
c	0.13	–	0.18
c1	0.12	0.127	0.134
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e		0.50BSC	
L	0.45	0.60	0.75
L1		1.00REF	
L2		0.25BSC	
R1	0.08	–	–
R2	0.08	–	0.20
S	0.20	–	–
θ	0°	3.5°	7°
θ1	0°	–	–
θ2	11°	12°	13°
θ3	11°	12°	13°

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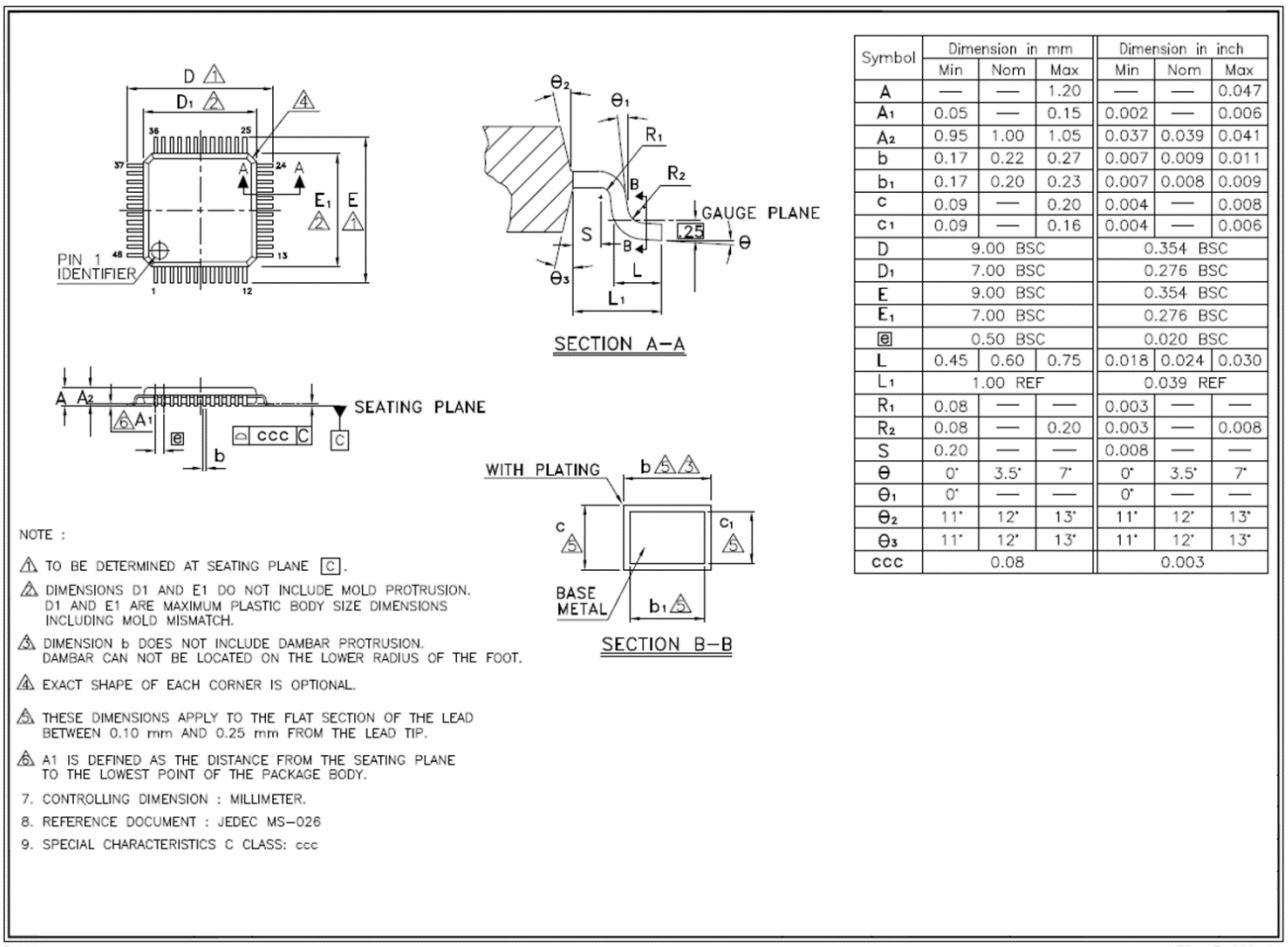
5.2 TQFP48

Figure 5-2 TQFP48 package outline



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.20	—	—	0.047
A1	0.05	—	0.15	0.002	—	0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
b	0.17	0.22	0.27	0.007	0.009	0.011
b1	0.17	0.20	0.23	0.007	0.008	0.009
c	0.09	—	0.20	0.004	—	0.008
c1	0.09	—	0.16	0.004	—	0.006
D	9.00 BSC			0.354 BSC		
D1	7.00 BSC			0.276 BSC		
E	9.00 BSC			0.354 BSC		
E1	7.00 BSC			0.276 BSC		
e	0.50 BSC			0.020 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
R1	0.08	—	—	0.003	—	—
R2	0.08	—	0.20	0.003	—	0.008
S	0.20	—	—	0.008	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
ccc	0.08			0.003		

NOTE :

1. TO BE DETERMINED AT SEATING PLANE C.
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.
4. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
5. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.25 mm FROM THE LEAD TIP.
6. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
7. CONTROLLING DIMENSION : MILLIMETER.
8. REFERENCE DOCUMENT : JEDEC MS–026
9. SPECIAL CHARACTERISTICS C CLASS: ccc

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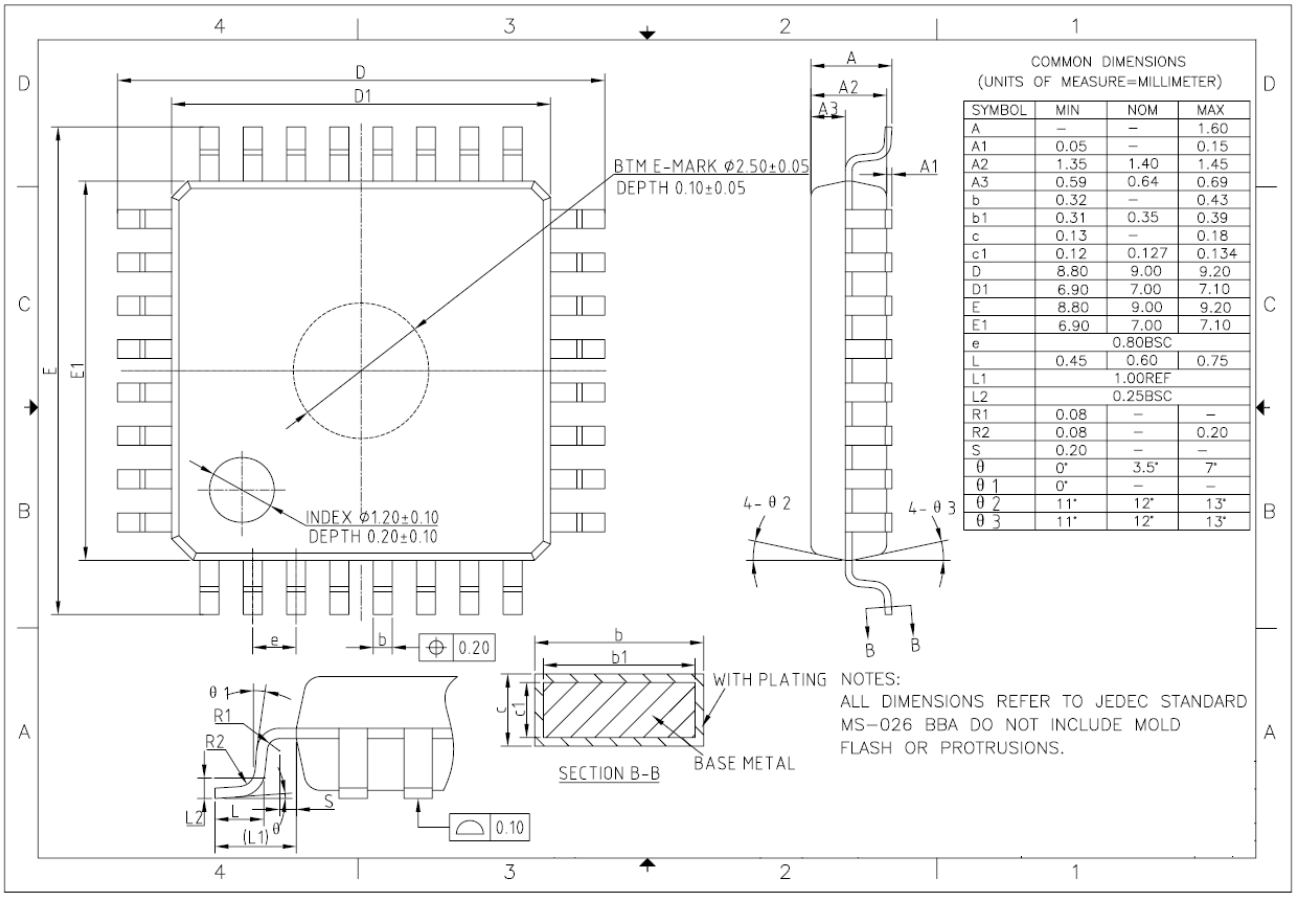
5.3 LQFP32

Figure 5-3 LQFP32 package outline



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.32	–	0.43
b1	0.31	0.35	0.39
c	0.13	–	0.18
c1	0.12	0.127	0.134
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e		0.80BSC	
L	0.45	0.60	0.75
L1		1.00REF	
L2		0.25BSC	
R1	0.08	–	–
R2	0.08	–	0.20
S	0.20	–	–
θ	0°	3.5°	7°
θ1	0°	–	–
θ2	11°	12°	13°
θ3	11°	12°	13°

NOTES:
ALL DIMENSIONS REFER TO JEDEC STANDARD MS-026 BBA DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

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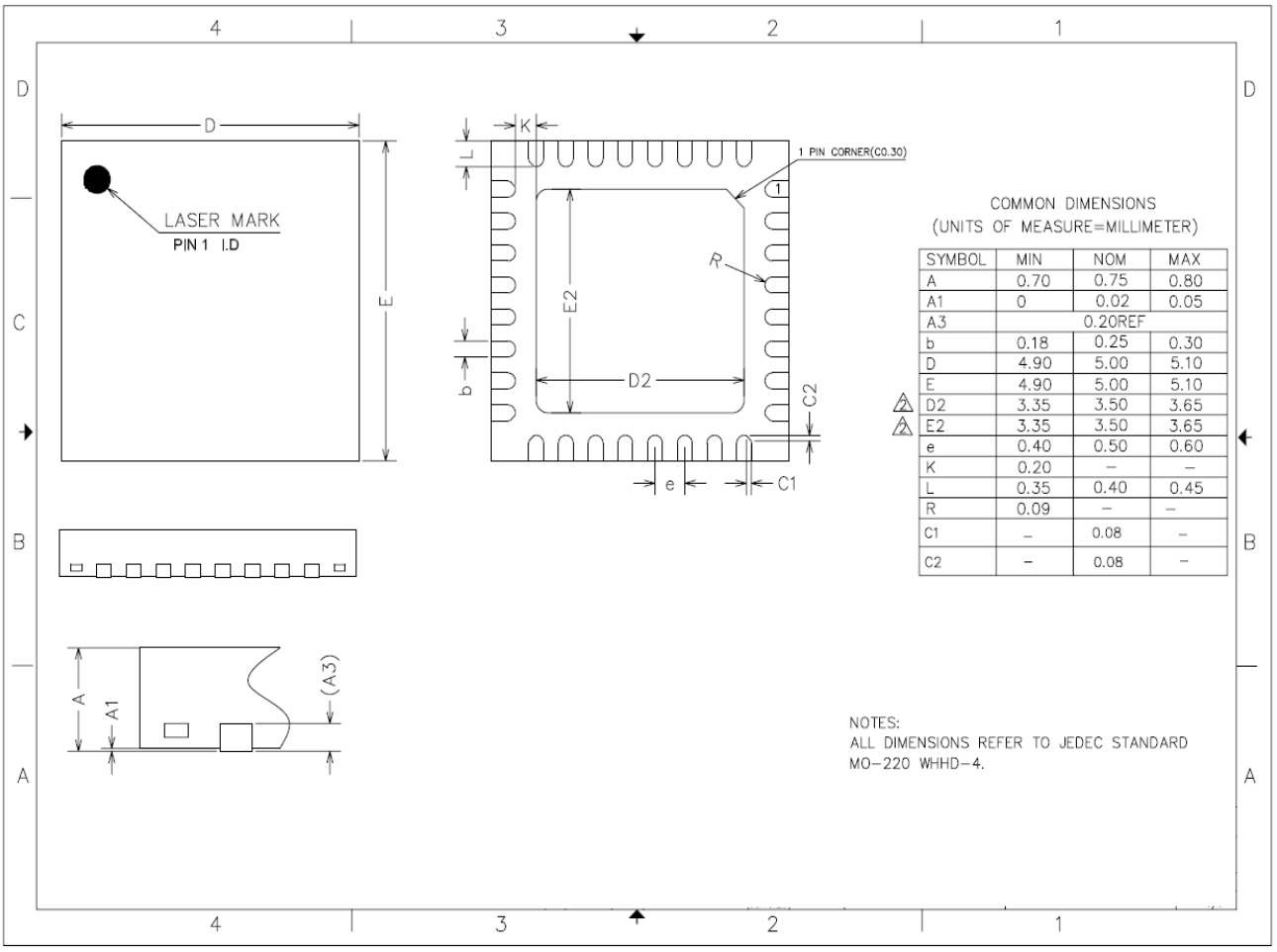
5.4 QFN32 (5mx5m)

Figure 5-4 QFN32 (5mx5m) package outline



SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
A3		0.20REF	
b	0.18	0.25	0.30
D	4.90	5.00	5.10
E	4.90	5.00	5.10
D2	3.35	3.50	3.65
E2	3.35	3.50	3.65
e	0.40	0.50	0.60
K	0.20	–	–
L	0.35	0.40	0.45
R	0.09	–	–
C1	–	0.08	–
C2	–	0.08	–

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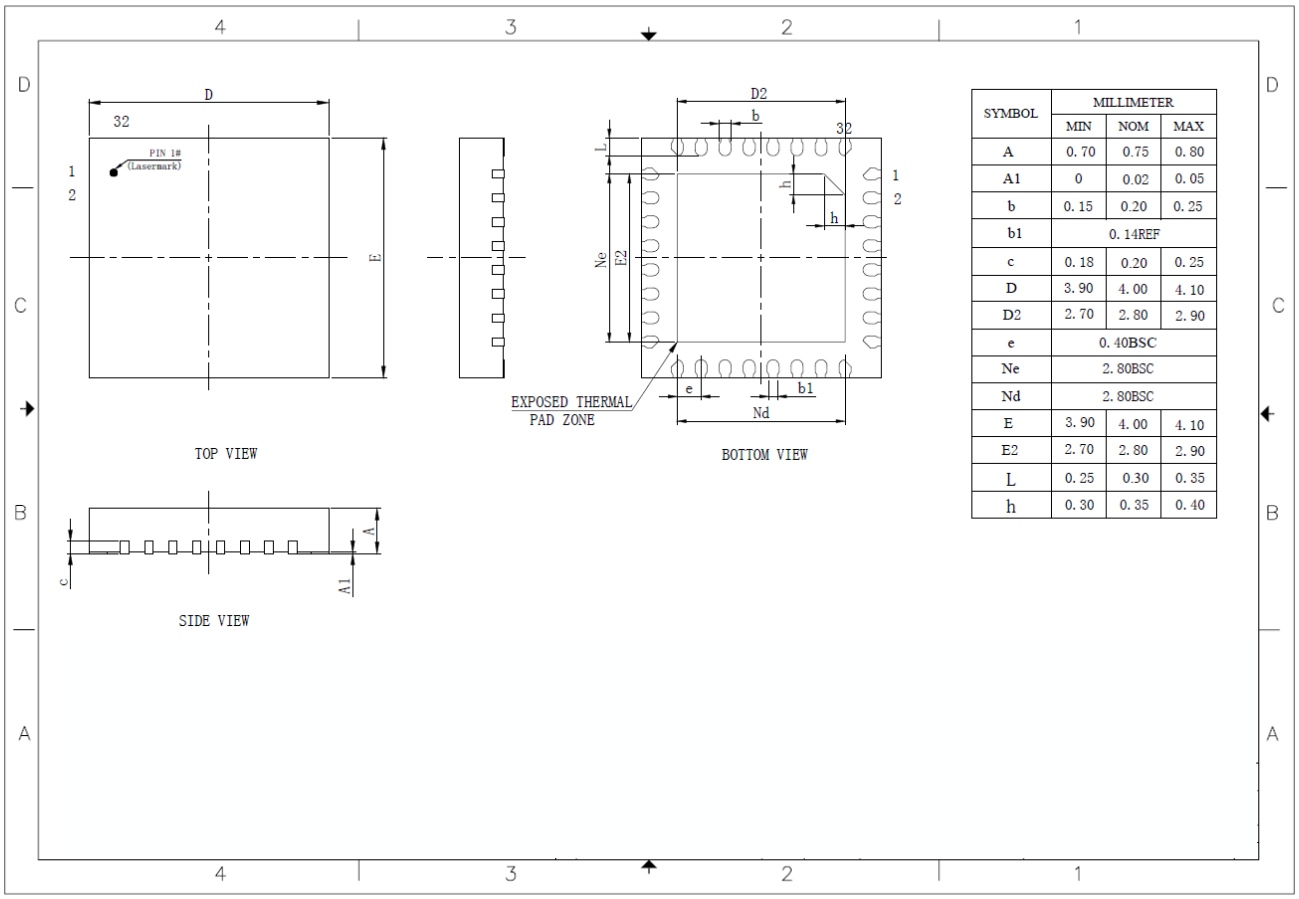
5.5 QFN32 (4mx4m)

Figure 5-5 QFN32 (4mx4m) package outline



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.15	0.20	0.25
b1		0.14REF	
c	0.18	0.20	0.25
D	3.90	4.00	4.10
D2	2.70	2.80	2.90
e		0.40BSC	
Ne		2.80BSC	
Nd		2.80BSC	
E	3.90	4.00	4.10
E2	2.70	2.80	2.90
L	0.25	0.30	0.35
h	0.30	0.35	0.40

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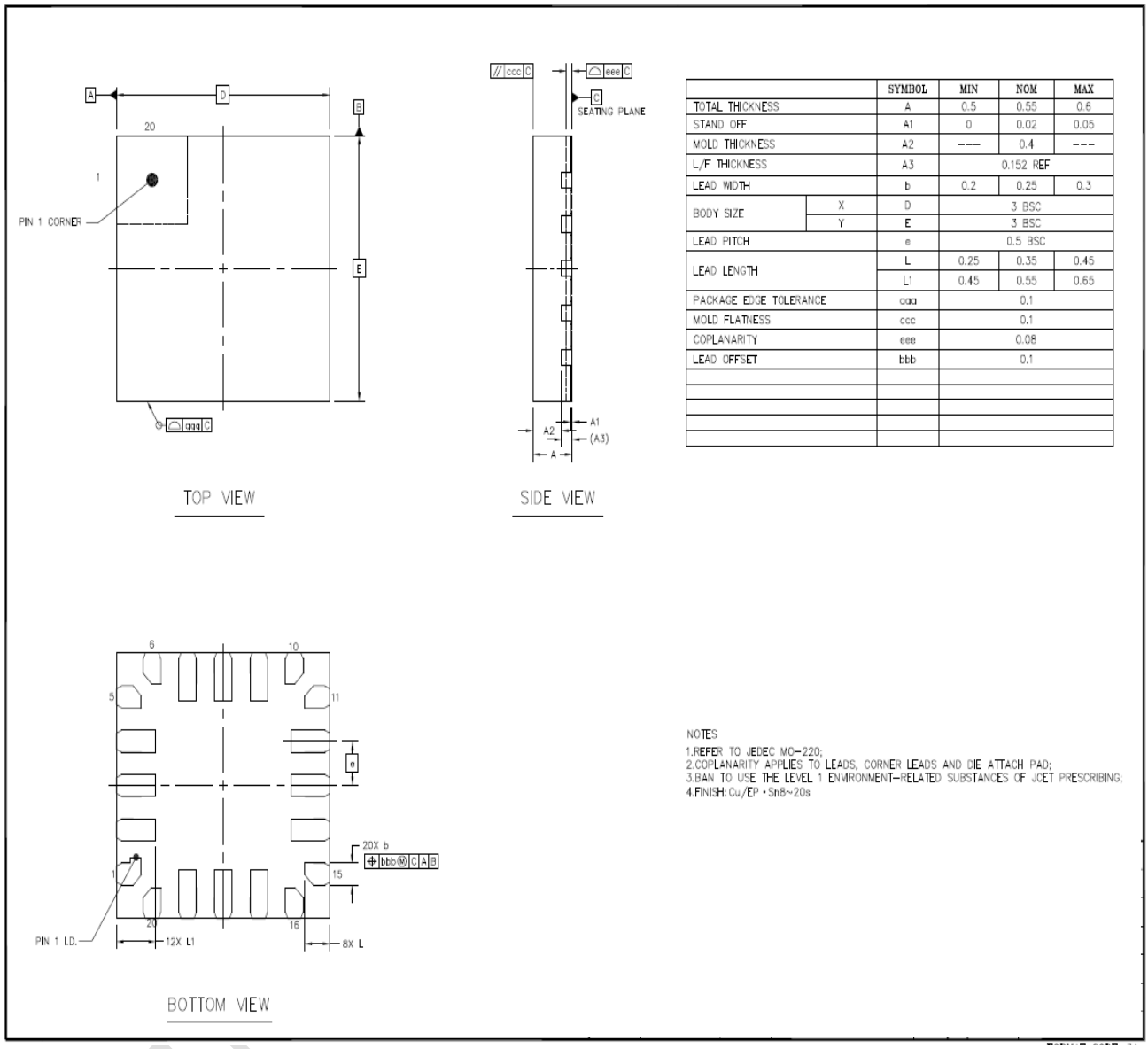
5.6 UFQFPN20

Figure 5-6 UFQFPN20 package outline



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.5	0.55	0.6
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.4	---
L/F THICKNESS		A3		0.152 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		3 BSC	
	Y	E		3 BSC	
LEAD PITCH		e		0.5 BSC	
LEAD LENGTH		L	0.25	0.35	0.45
		L1	0.45	0.55	0.65
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.1	

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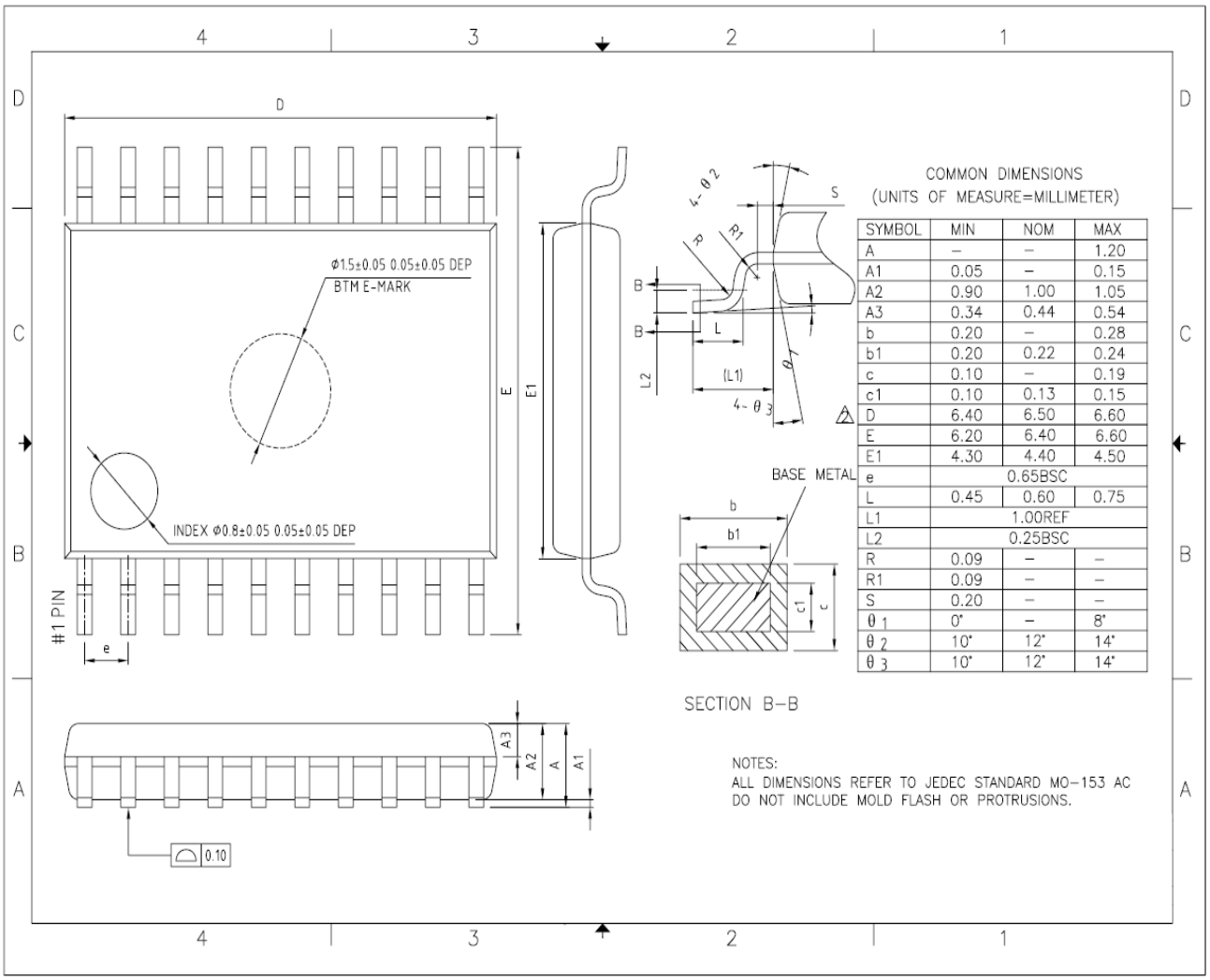
5.7 TSSOP20

Figure 5-7 TSSOP20 package outline



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.20
A1	0.05	–	0.15
A2	0.90	1.00	1.05
A3	0.34	0.44	0.54
b	0.20	–	0.28
b1	0.20	0.22	0.24
c	0.10	–	0.19
c1	0.10	0.13	0.15
D	6.40	6.50	6.60
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00REF		
L2	0.25BSC		
R	0.09	–	–
R1	0.09	–	–
S	0.20	–	–
θ 1	0°	–	8°
θ 2	10°	12°	14°
θ 3	10°	12°	14°

NOTES:
ALL DIMENSIONS REFER TO JEDEC STANDARD MO-153 AC
DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

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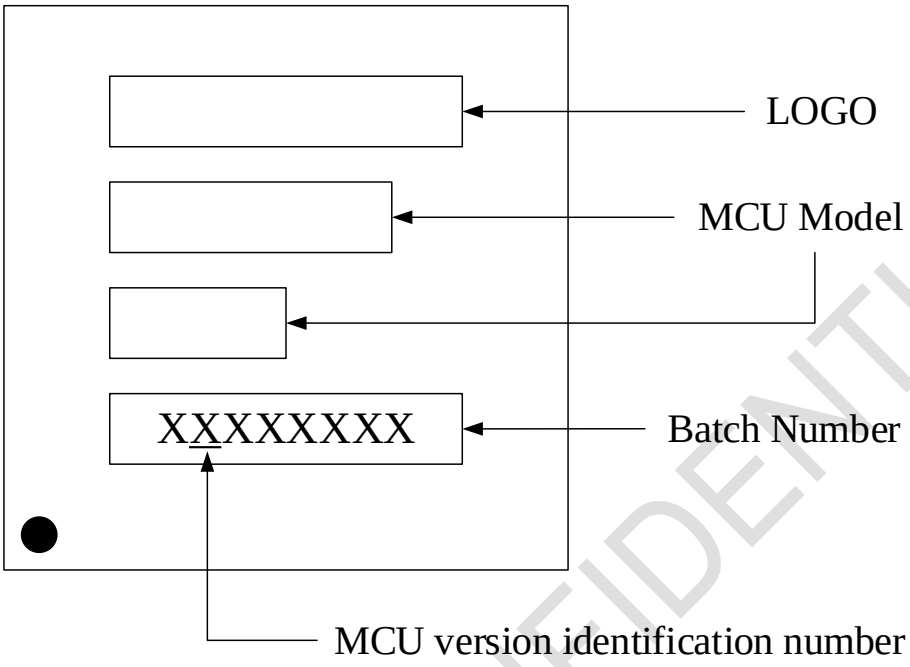
5.8 Screen printing instructions

Figure 5-8 Screen printing instructions



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6 Revision History

Date	Revision No.	Description
2021.11.08	V1.0.0	Initial version
2021.11.11	V1.0.1	Modify Figure 1-2 Modify Figure 4-17 Modify Table 1-1 Modify Table 1-2

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